Title: Low-overhead fault-tolerant quantum computing with high-rate qLDPC codes

Speakers: Xian Qu

Collection/Series: Quantum Information

Subject: Quantum Information

Date: February 05, 2025 - 11:00 AM

URL: https://pirsa.org/25020028

Abstract:

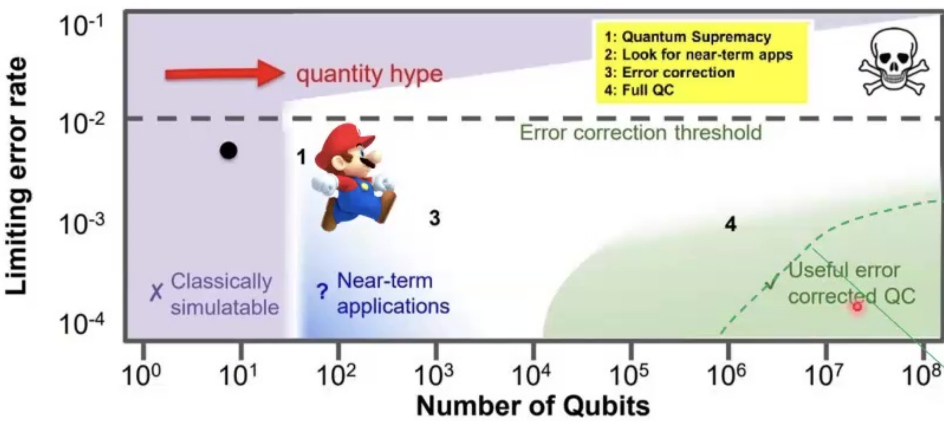
High-rate quantum low-density parity-check (qLDPC) codes offer significantly lower encoding overhead compared to their topological counterparts by relaxing locality constraints. However, achieving full-fledged logical computation with these codes in physical systems with low space-time costs remains a formidable challenge. In the first part of this talk, I will provide an overview of recent advancements in implementing qLDPC codes as quantum memories on realistic platforms, such as reconfigurable atom arrays. Next, I will present a new scheme for performing parallelizable and locally addressable logical operations on homological product codes. This scheme extends the transversal CNOT gate from two identical CSS codes to two distinct, yet structurally similar, qLDPC codes, enabling efficient local addressing of collectively encoded information. We demonstrate that this approach achieves lower overhead in not only the space- but also the overall space-time overhead compared to surface-code-based computations. Finally, I will discuss new strategies for achieving highly space-time-efficient computations with qLDPC codes by leveraging algorithm-specific fault tolerance, designing tailored protocols for structured quantum algorithms.

Low-overhead fault-tolerant quantum computing with high-rate qLDPC codes

Qian Xu
Postdoctoral fellow @ Caltech

@ Perimeter Institute, 02/05/2025

Fault-tolerant quantum computing? Mind the gap!



Cr: John Martinis

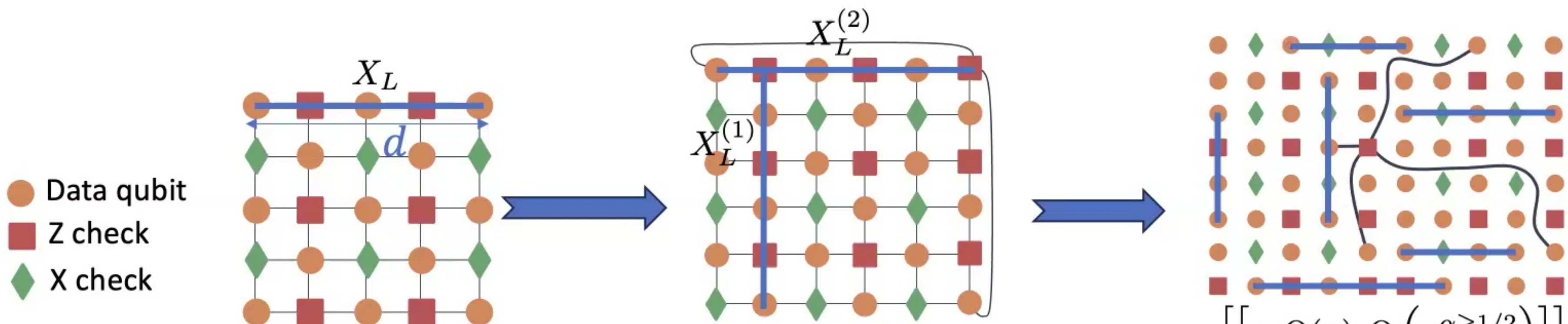
Surface codes

Google Quantum AI, Nature (2023); D. Litinski, Quantum (2019)

2

Bridge the gap with high-rate qLDPC codes

➢ Large space overhead of topological codes (2D- or 3D-logcal)

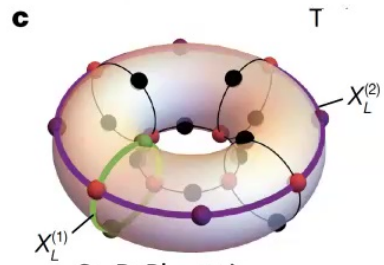


$[[n, k = 1, d = \sqrt{n}]]$ $[[n, 2, \sqrt{n}]]$ $\left[\left[n, \Theta(n), \Theta\left(n^{\alpha \geq 1/2}\right)\right]\right]$

$n/k = d^2 \sim \mathbf{1000}$

- Connectivity constrains quantum codes!
- BPT bound (2D): $kd^2 \leq O(n)$

S. Bravyi, D. Poulin, and B. Terhal, *Phys. Rev. Lett.* (2010)



Cr: D. Bluvstein

➢ High-rate qLDPC codes:
constant space overhead

[1]. Gottesman, *arXiv* 1310.2984 (2013)
[2]. Breuckmann and Eberhardt, *PRX Quantum* (2021)
[3]. Panteleev and Kalachev, *arXiv* 2111.03654 (2021)
......

Challenges

Low-overhead FTQC with qLDPC codes?

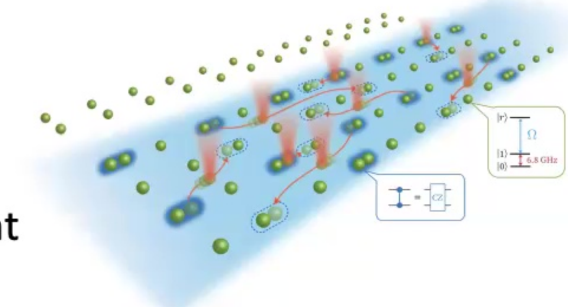
- Physical implementation
- Locally addressable and parallelizable logical gates
- FTQC with low space-time overhead

Challenges

Low-overhead FTQC with qLDPC codes?

- **Physical implementation**
- Locally addressable and parallelizable logical gates
- FTQC with low space-time overhead

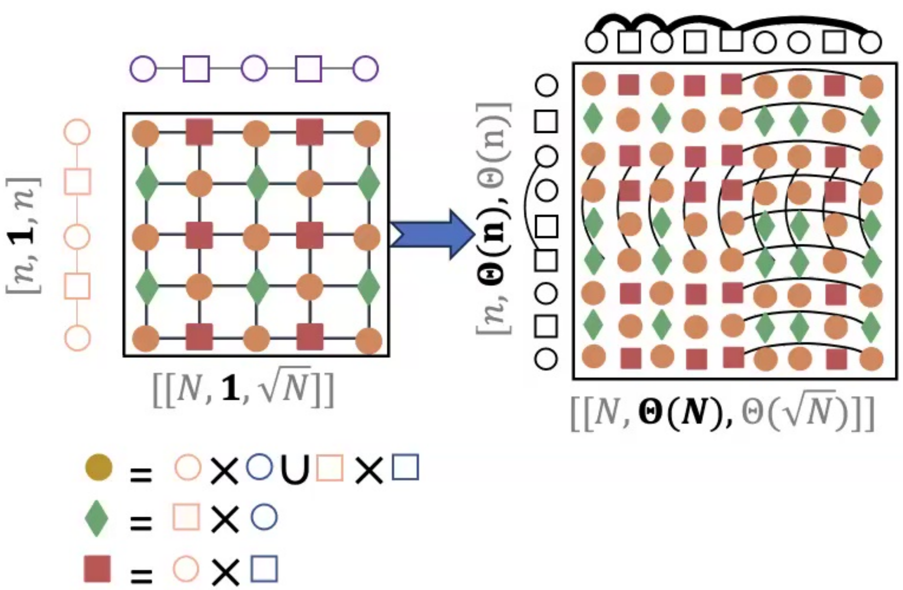
qLDPC implementation



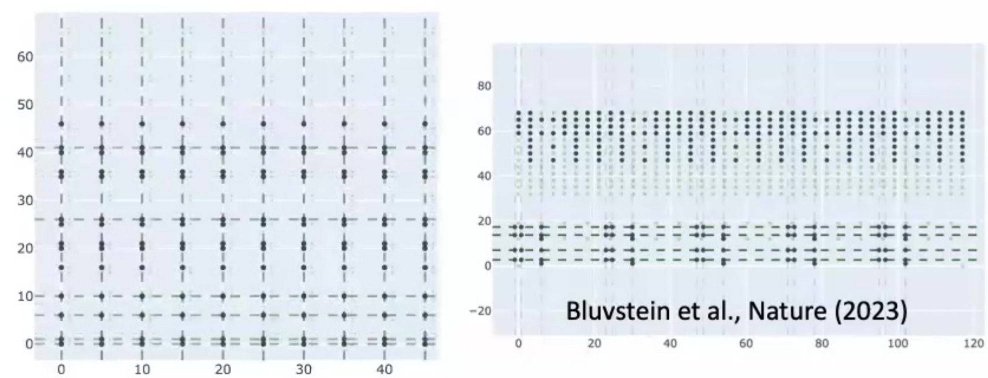
➢ Implementation of "**product**" codes with **global 1D** atom rearrangement

- Hypergraph product (HGP) codes

  Tillich and Zemor, IEEE Trans. Inf. Theory (2014)



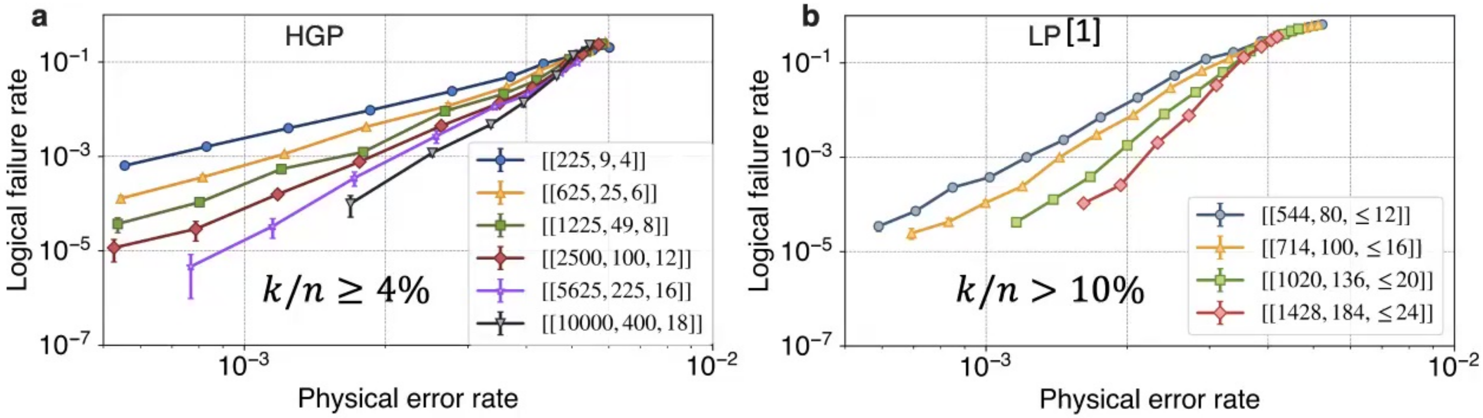
- "Product Coloration" syndrome extraction via **row/column permutation**



- Generalizes to other product codes, e.g. lifted products

Q. Xu*, P. Bonilla* et al. *Nat. Phys* (2024) 6

qLDPC implementation



❖ High Pseudo-threshold p_{th}~**0.6%** and low logical failure rates at $p_g = 10^{-3}$

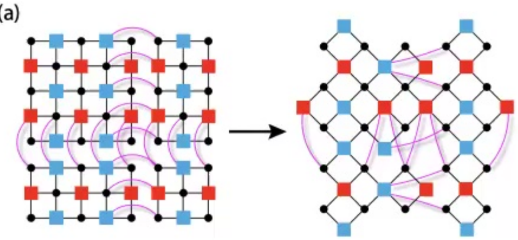
Logical qubits	25	80	180	400
Logical failure rate	10^{-3}	10^{-4}	2×10^{-5}	6×10^{-6}
HGP code physical qubits (improvement over surface code)	1235 (1×)	4606 (2.8×)	10760 (4.0×)	19600 (6.9×)
LP code physical qubits (improvement over surface code)	851 (1.4×)	1367 (9.4×)	2670 (16.2×)	

[1] Panteleev & Kalachev, *IEEE Trans. Inf. Theory* (2022).

Q. Xu*, P. Bonilla* et al. *Nat. Phys* (2024)

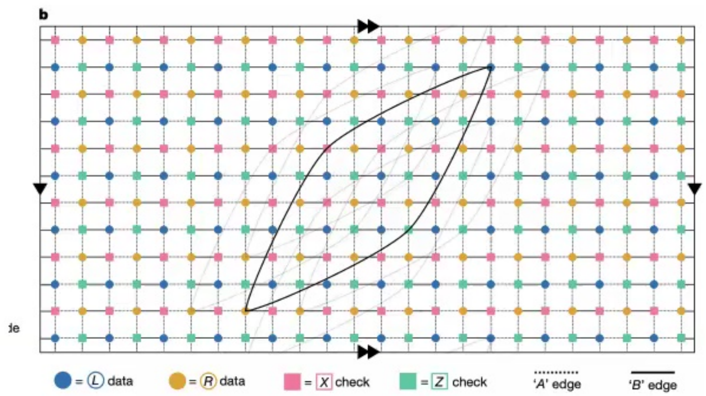
qLDPC implementation

(a)



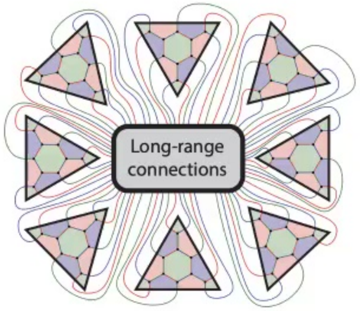
Long-range enhanced surface codes with ion shuttling

Y. Hong et al., Phys. Rev. Lett. (2024)



Bivariate bicycle codes with bilayer superconducting architectures

S. Bravyi et al., Nature (2024)



Hyperbolic codes with modular architectures

O. Higgott & N. Breuckmann., PRX Quantum (2024)

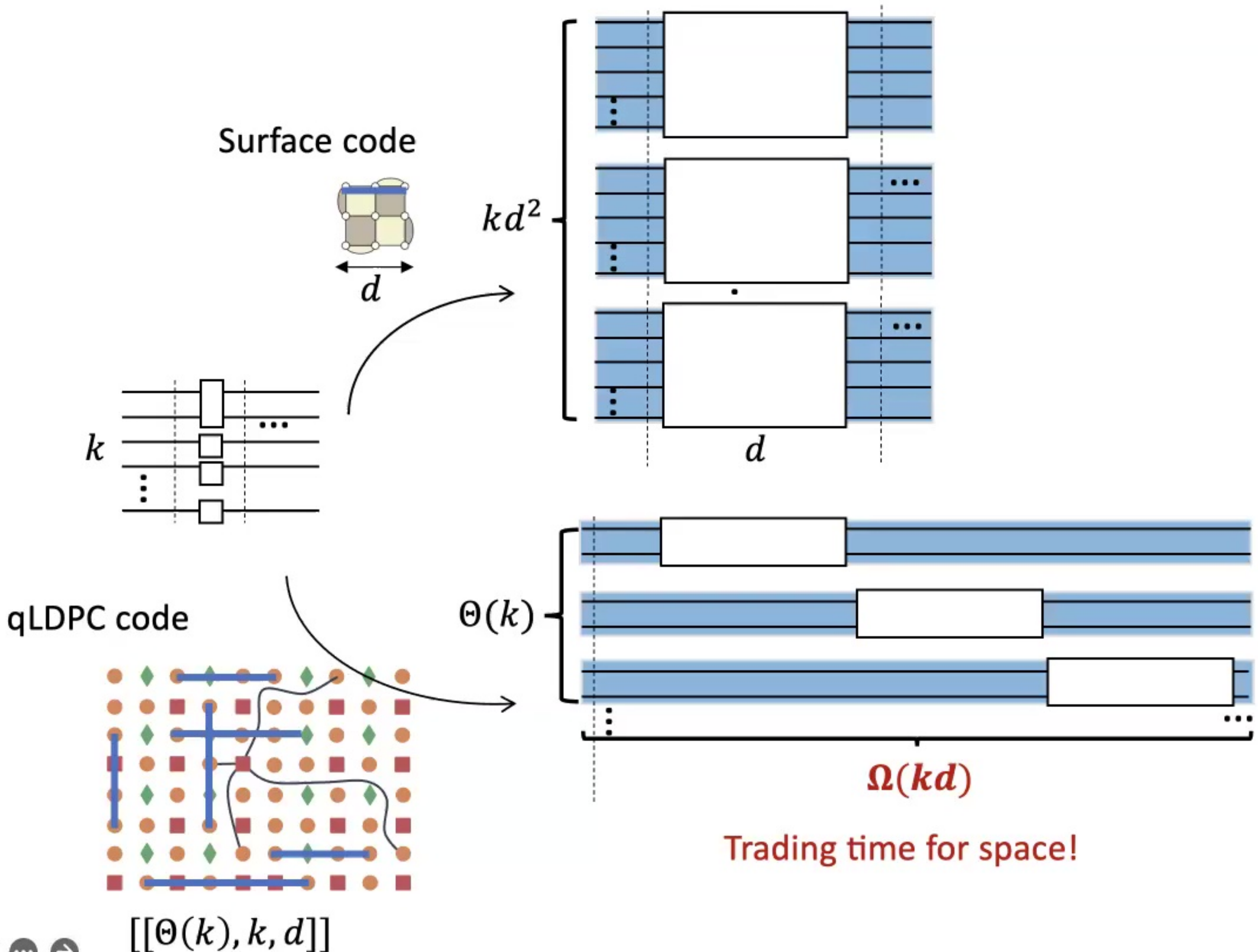
❖ Take home: promising implementation of finite-size qLDPC codes by co-designing the codes and the hardware

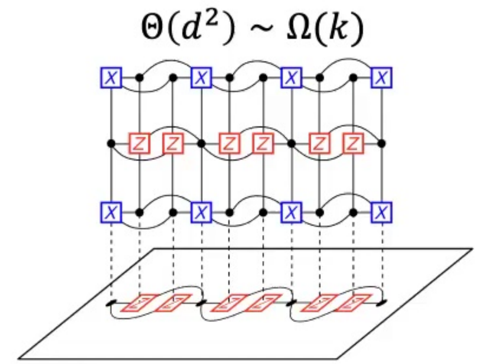
Challenges

Low-overhead FTQC with qLDPC codes?

- Physical implementation
- **Locally addressable and parallelizable logical gates**
- FTQC with low space-time overhead

Addressable and parallelizable logical gates





Lattice (LDPC) surgeries

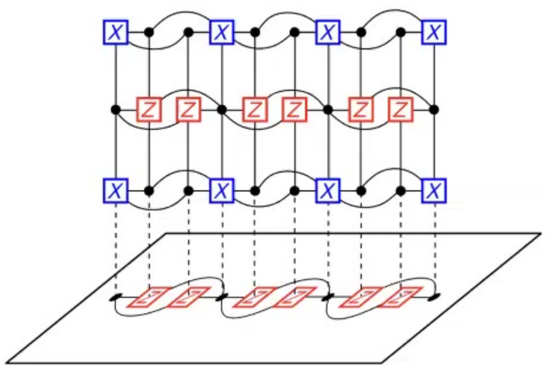
Cohen et al., *Science Advances* (2021)

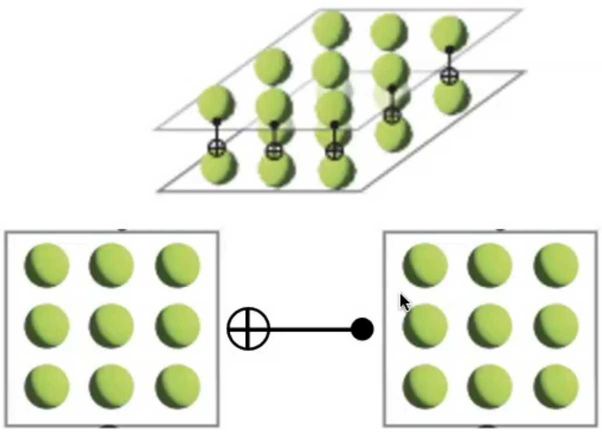
*Improved:

- Cross et al., *arXiv* 2407.18393 (2024).
- Williamson et al., *arXiv* 2410.02213 (2024).
- Ide et al., *arXiv* 2410.02753 (2024).

...

Addressable and parallelizable logical gates



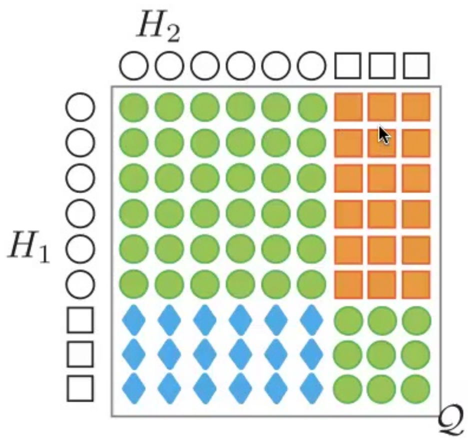


- Lattice surgery with rateless ancillae
  - Addressable ✓
  - Parallelizable ✕

- Transversal CNOTs and Steane measurement
  - Addressable ✕
  - Parallelizable ✓

Q. Xu et al. *arXiv* 2407.18490 (2024) 11

Homomorphic gadgets for homological product codes

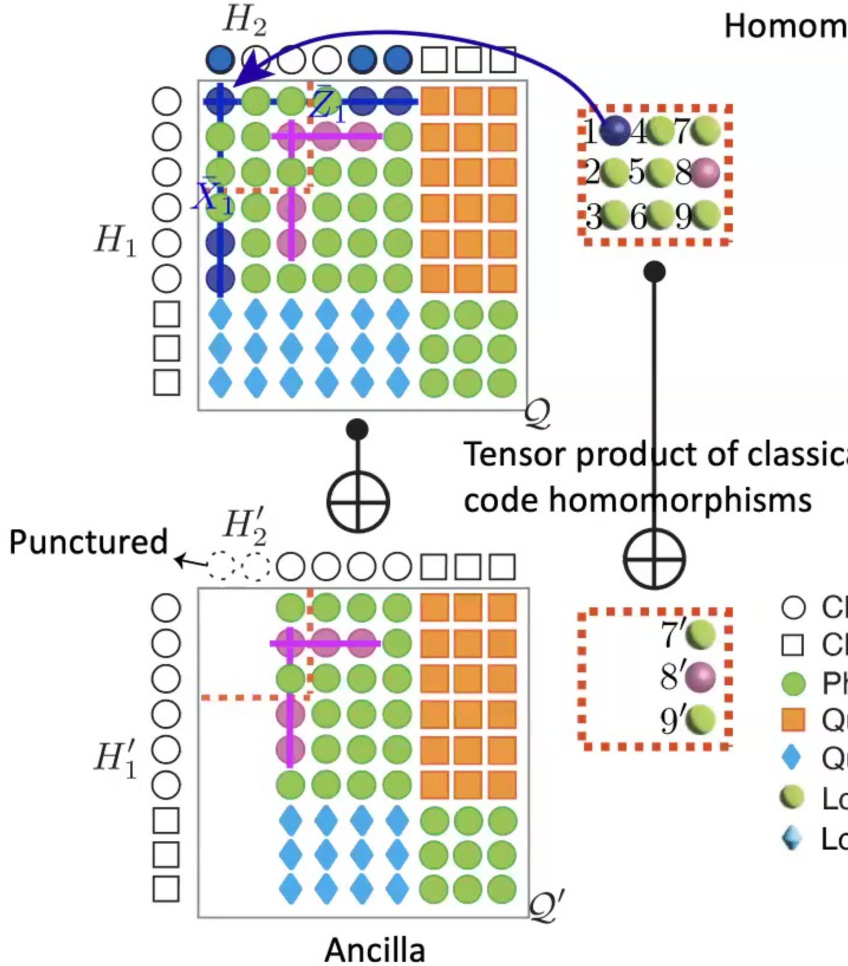


Hypergraph product code [1]

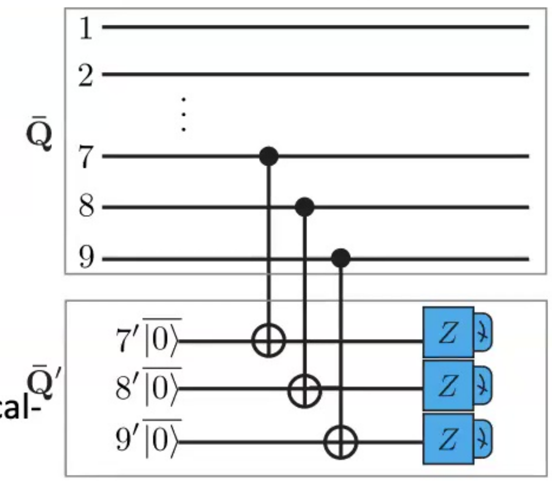
[1]. Tillich & Zemor., *IEEE T. Inf. Theory* (2014)

Q. Xu et al. *arXiv* 2407.18490 (2024) 12

Homomorphic gadgets for homological product codes



Homomorphic measurements (generalized Steane measurements)



- **Naturally fault-tolerant**
  - Maintain LDPC
  - Large-distance ancilla
  - Transversal gates and measurements.
  - FT state prep
- **Selective and parallel**

14

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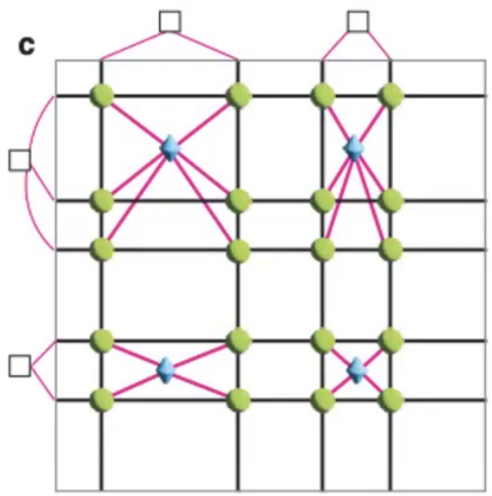
Parallel Pauli-product measurements for HGP codes

➢ "Grid Pauli-product measurements" (GPPMs):



GPPMs

- $O(1)$ space overhead, in 1 logical cycle (d code cycles)

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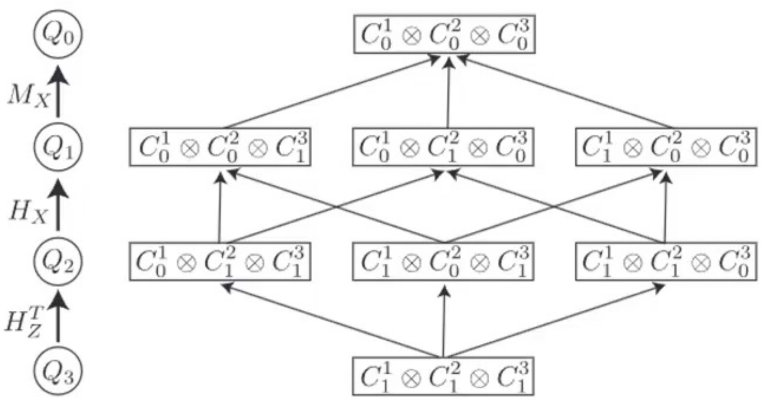
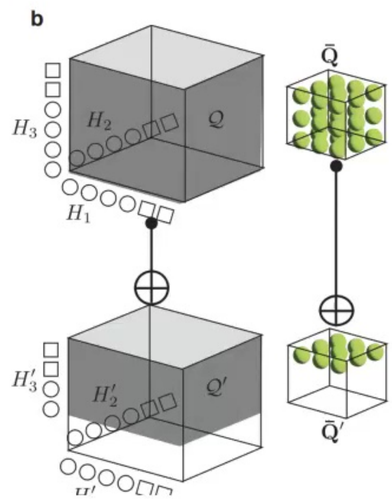
Constant-depth gadgets with 3D/4D homological product codes



$M_X H_X = 0$

Meta checks



- Single-shot state prep due to soundness [1]
- "Cube" PPMs with constant space-time overhead

[1]. Campbell, *Quantum Science and Technology* (2019)

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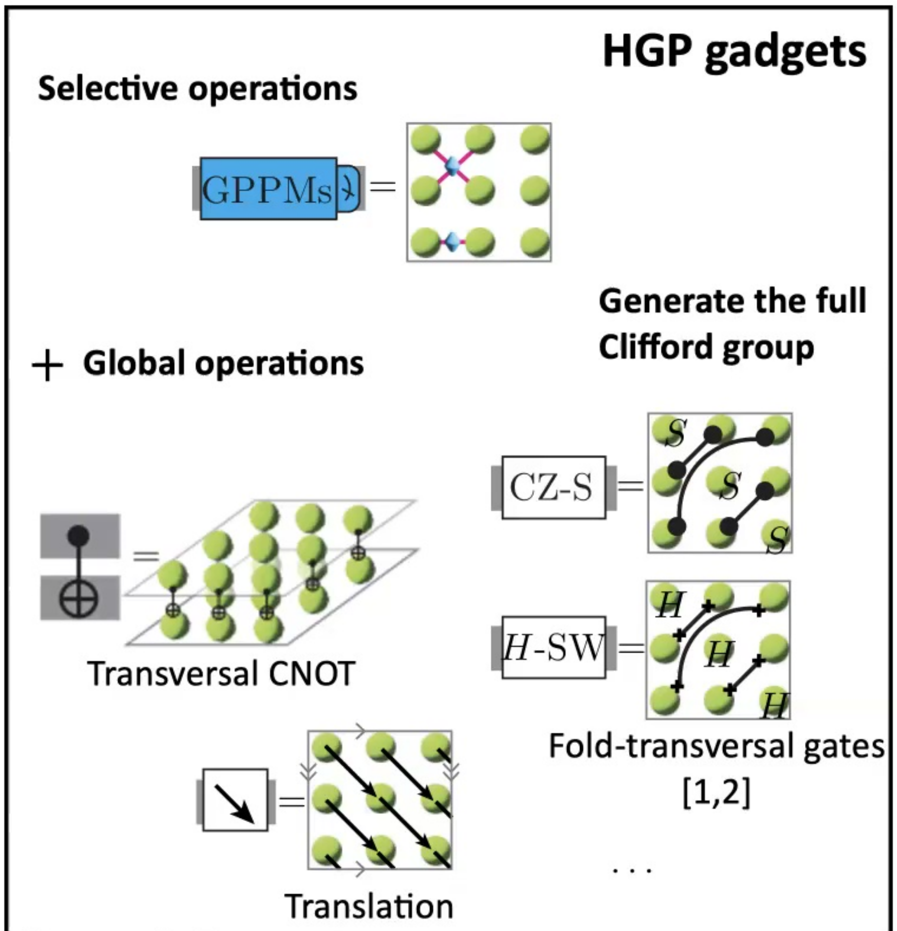
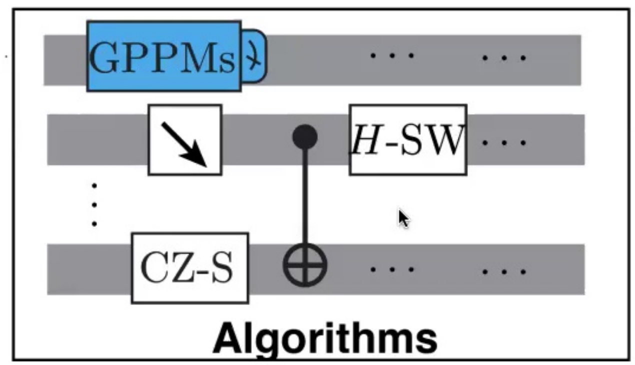
Universal & parallel computation with HGP codes



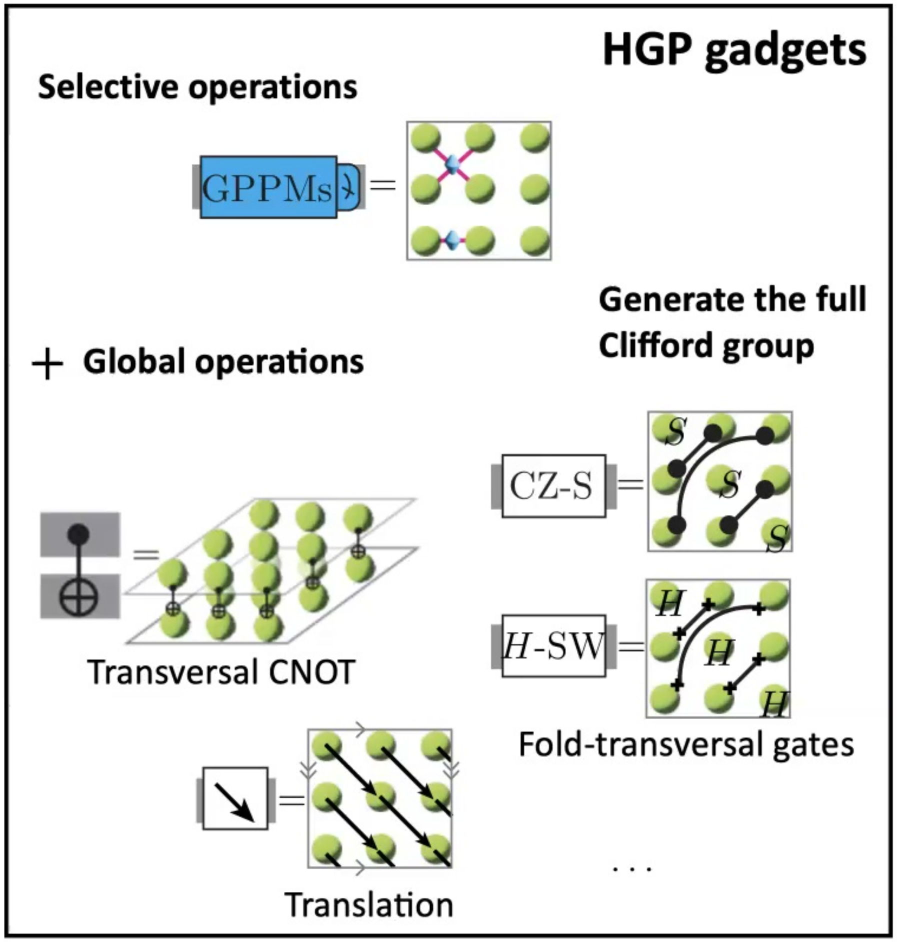


With lower space-time overhead over surface-code computations?

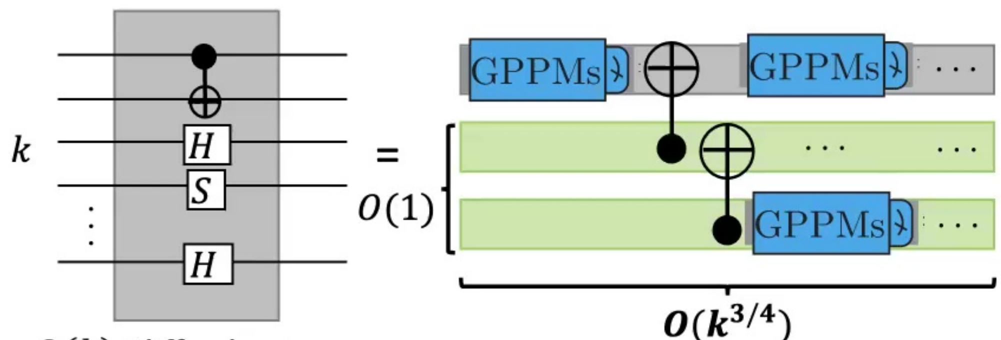
[1]. Breuckmann et al., *Quantum* (2024).
[2]. Quintavalle. et al., *Quantum* (2023).

Q. Xu et al. *arXiv* 2407.18490 (2024)

Universal & parallel computation with HGP codes



- Parallel intra-block operations



$\Theta(k)$ Clifford gates

Lower space-time overhead than surface codes (with lattice surgery)

Q:

- Can we do better than $O(k^{3/4})$?
- Logical computations with significantly lower overhead?

Q. Xu et al. *arXiv* 2407.18490 (2024) 18

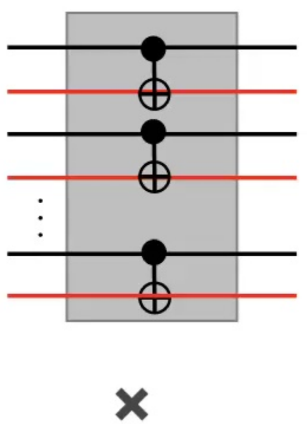
Challenges

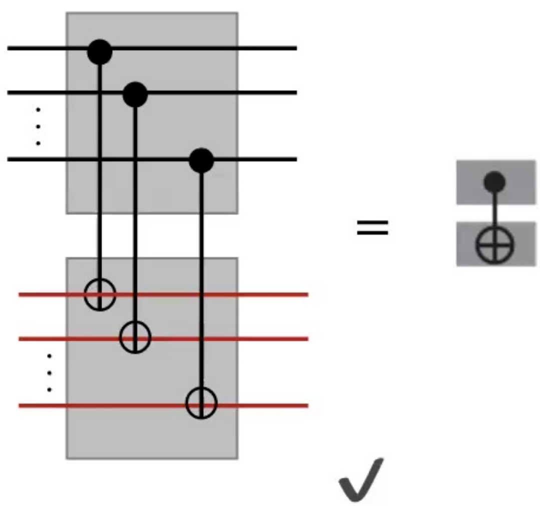
Low-overhead FTQC with qLDPC codes?

- ➢ Physical implementation
- ➢ Locally addressable and parallelizable logical gates
- ➢ **FTQC with low space-time overhead**

Parallel computation with HGP codes

➢ **Algorithm-specific compilation**

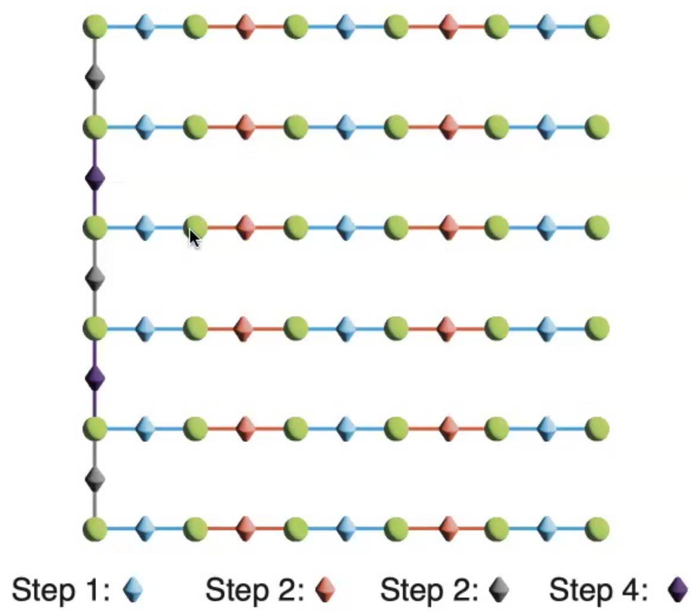




- Compile algorithms into structured layers of gates more compatible with the native HGP gadgets
- Leverage parallel inter-block operations
- Minimize selective intra-block operations
- "Many logical qubits are doing the same thing"

Parallel computation with HGP codes

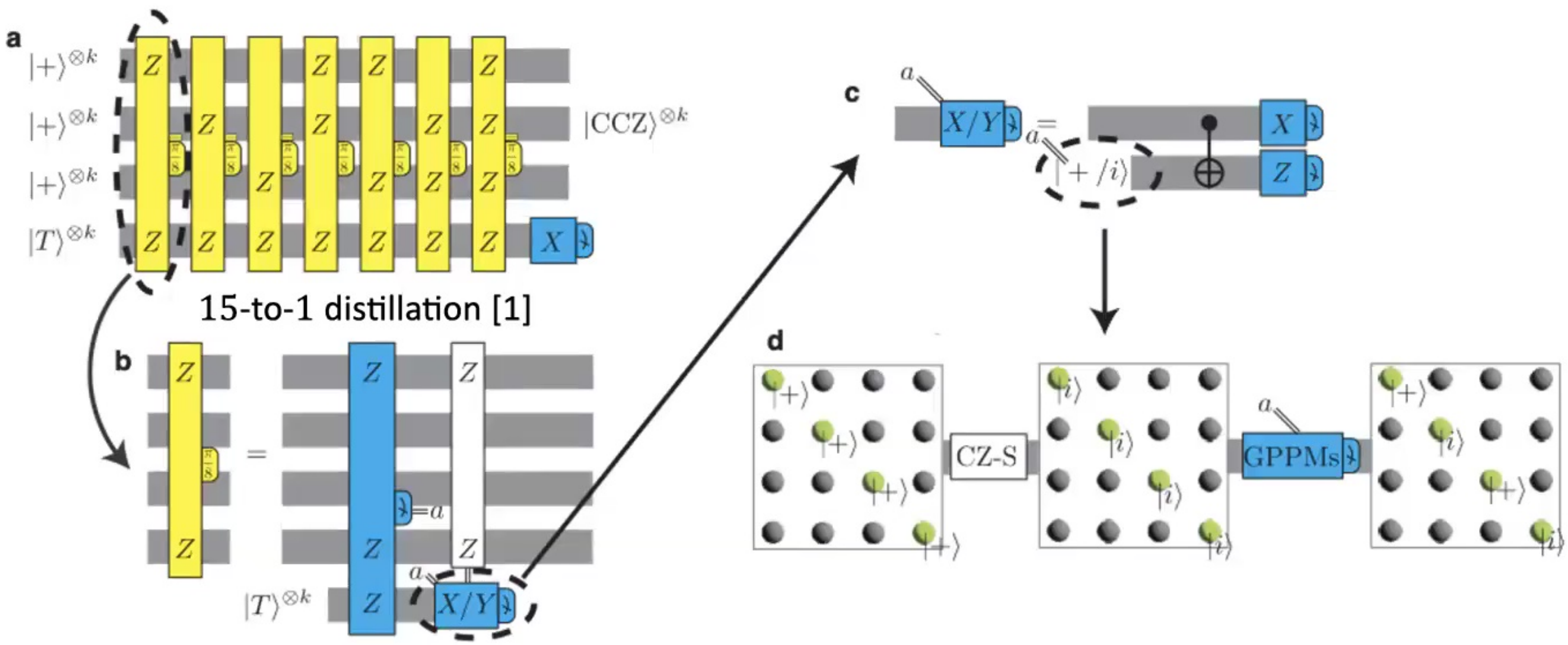
- Example 1: Logical GHZ state generation - $O(1)$ logical cycles



Q. Xu et al. arXiv 2407.18490 (2024) 21

Parallel computation with HGP codes

- Example 2: Magic state distillation - $O(\sqrt{k}\,\log k)$ logical cycles



[1]. Litinski et al., Quantum, (2019).

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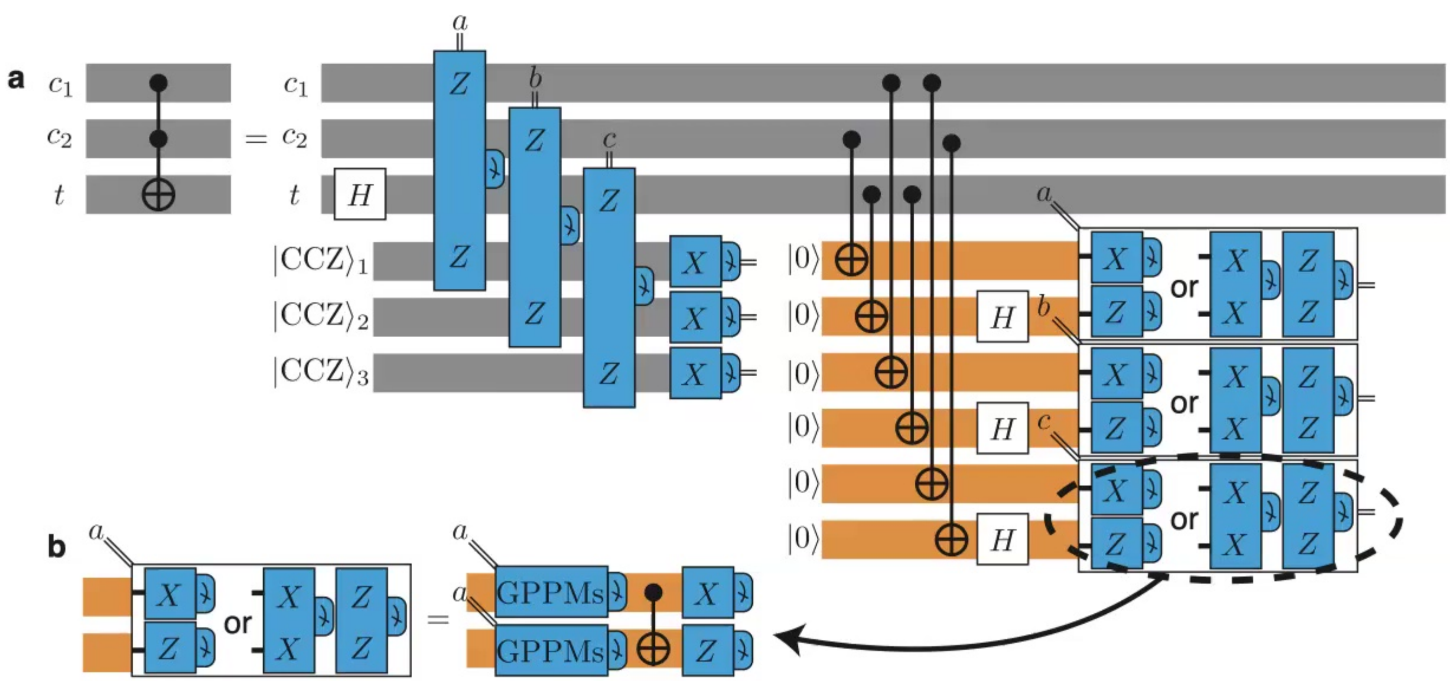
Parallel computation with HGP codes

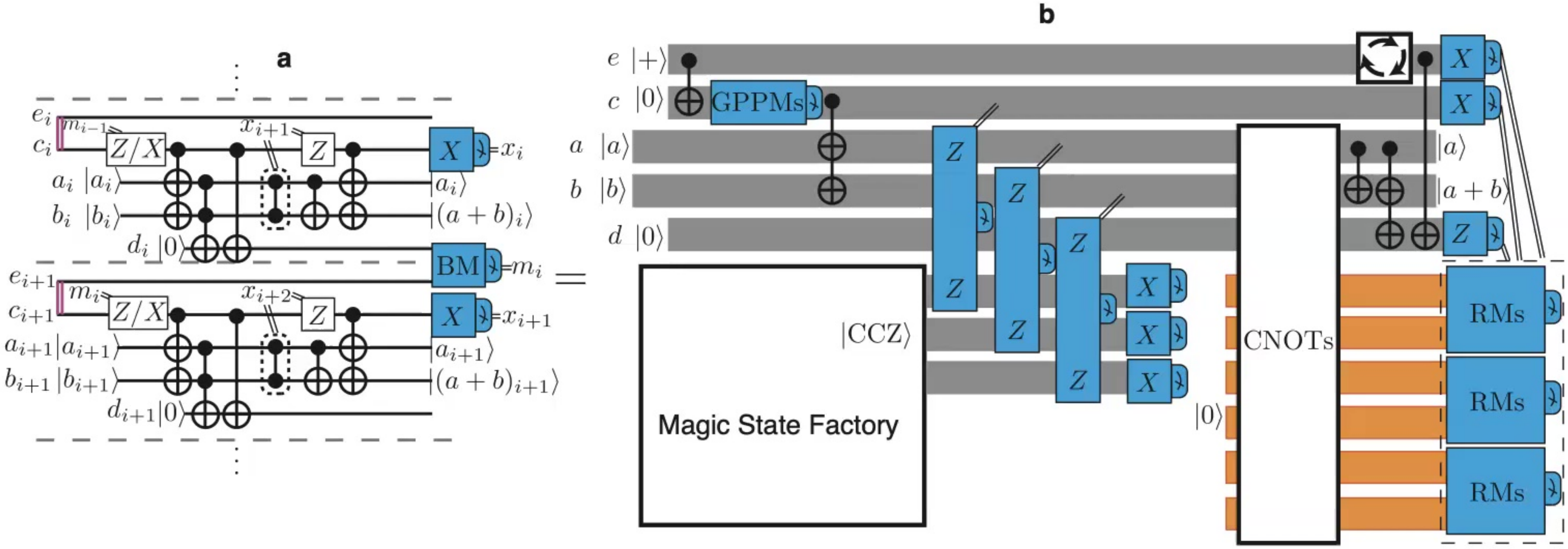
- Example 3: Magic state teleportation - $O(\sqrt{k}\log k)$ logical cycles



Q. Xu et al. arXiv 2407.18490 (2024) 23

Parallel computation with HGP codes

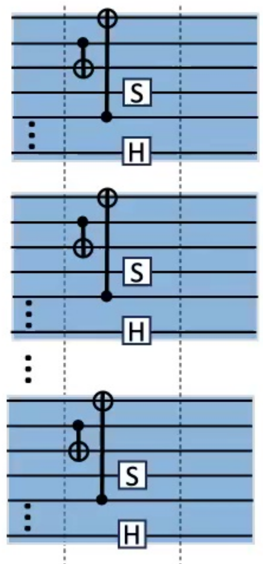
- Example 4: Quantum addition - $O(\sqrt{k}\,\log k)$ logical cycles



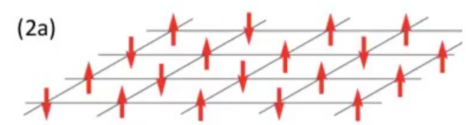
Q. Xu et al. arXiv 2407.18490 (2024) 24

Space-time efficient implementation of structured algorithms

- Result 1: **Arbitrary** parallel local Cliffords for **any** qLDPC codes **in bulk** with a **constant space-time overhead**



Structured quantum algorithms:



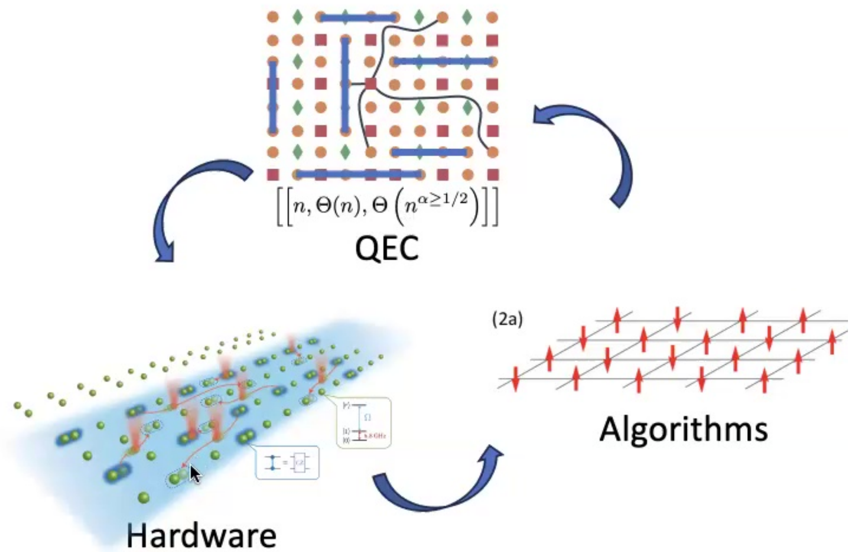
Quantum simulation of lattice Hamiltonians

- Result 2: Parallel high-fidelity magic state preparation & efficient Cliffords for self-dual bivariate bicycle codes with error rates $\sim 10^{-6}$

Q. Xu*, N. Maskara* et al. (in preparation)

Conclusion:

- Physical implementation of structured qLDPC codes by leveraging new hardware features, e.g. reconfigurable atom arrays.
- New schemes for performing locally addressable and parallelizable logical gates for homological product codes
- Space-time efficient FTQC using algorithm-specific FT protocols.



Outlook:

- Generalize the homomorphic gadgets for better qLDPC codes, e.g. lifted-product codes [1], generalized bicycle codes [2], etc.
- Reduce the logical cycle using correlated decoding & algorithmic fault tolerance [3,4].
- Co-design and algorithm-specific fault tolerance.

[1]. Panteleev & Kalachev, *Quantum* (2021).
[2]. Bravyi et al., *Nature* (2024).
[3]. Cain et al., arXiv 2403.03272 (2024).
[4]. Zhou et al., arXiv 2406.17653 (2024).

Thank you!

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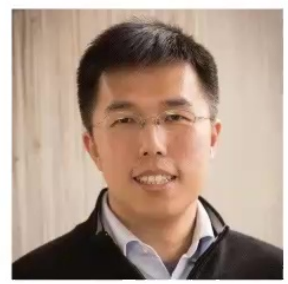

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Among others