Title: Concatenate codes, save qubits Speakers: Hayata Yamasaki Series: Perimeter Institute Quantum Discussions Date: April 10, 2024 - 11:00 AM

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Abstract: The essential requirement for fault-tolerant quantum computation (FTQC) is the total protocol design to achieve a fair balance of all the critical factors relevant to its practical realization, such as the space overhead, the threshold, and the modularity. A major obstacle in realizing FTQC with conventional protocols, such as those based on the surface code and the concatenated Steane code, has been the space overhead, i.e., the required number of physical qubits per logical qubit. Protocols based on high-rate quantum low-density parity-check (LDPC) codes gather considerable attention as a way to reduce the space overhead, but problematically, the existing fault-tolerant protocols for such quantum LDPC codes sacrifice the other factors. Here we construct a new fault-tolerant protocol to meet these requirements simultaneously based on more recent progress on the techniques for concatenated codes rather than quantum LDPC codes, achieving a constant space overhead, a high threshold, and flexibility in modular architecture designs. In particular, under a physical error rate of 0.1%, our protocol reduces the space overhead to achieve the logical CNOT error rates 10^{-10} and 10^{-24} by more than 90% and 97%, respectively, compared to the protocol for the surface code. Furthermore, our protocol achieves the threshold of 2.4% under a conventional circuit-level error model, substantially outperforming that of the surface code. The use of concatenated codes also naturally introduces abstraction layers essential for the modularity of FTQC architectures. These results indicate that the code-concatenation approach opens a way to significantly save qubits in realizing FTQC while fulfilling the other essential requirements for the practical protocol design.

Zoom link

Concatenate codes, save qubits

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References:

Hayata Yamasaki, Masato Koashi, <u>arXiv:2207.08826</u> Nature Physics 2024 Satoshi Yoshida, Shiro Tamiya, Hayata Yamasaki, <u>arXiv:2402.09606</u>

About Me

Social	Advance of IT society				
implementation by quantum technology					
	Useful quantum algorithm				
	Quantum machine learning				
	with high speed/applicability				
<u>Theoretical</u>	Implementation of QC				
foundation	Low-overhead/scalable				
<u>= my works</u>	fault-tolerant QC (FTQC)				
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	Efficient Q operations				
	Quantitative analysis of use				
	of quantum resources				
Experimental	Advance of				
foundation	quantum technology				

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- **Provable quantum advantage** in solving machine learning tasks <u>arXiv:2305.11212</u>, <u>arXiv:2312.03057</u>
- Quantum machine learning (QML) using exponential speedup without sparse or low-rank matrices arXiv:2004.10756 (NeurIPS2020), arXiv:2106.09028 arXiv:2301.11936 (ICML2023)
- Time-efficient constant-space-overhead FTQC arXiv:2207.08826 (Nat.Phys.2024) arXiv:2402.09606
- Analysis of GKP Code <u>arXiv:1910.08301 (PRA2020)</u> <u>arXiv:1911.11141 (PRR2020)</u> <u>arXiv:2006.05416</u>
- Practical testing of entangled states <u>arXiv:2201.11127</u> <u>arXiv:2202.13131 (PRL2022)</u>
- Quantum resource theories <u>arXiv:2310.09154 (PRL2024)</u>
 <u>arXiv:2106.01372 (Quantum2022)</u> etc.



<u>**Task</u>**: Given ϵ and an original circuit, perform **the noisy circuit** to output $x \sim \tilde{p}(x) \approx_{\epsilon} p(x)$ (the fault-tolerant circuit)</u>

→ Use quantum error-correcting codes that can suppress logical error rate arbitrarily

 $p_0 < p_{th} \Rightarrow p_L \lessapprox \frac{\epsilon}{WD}$ for achieving the overall error $O(\epsilon)$ Below threshold Width × Depth = Circuit size Space overhead := $\frac{W_{FT}}{W}$ Time overhead := $\frac{D_{FT}}{D}$ Yamasaki, Koashi, arXiv:2207.08826 (Nat. Phy. 2024), Yoshida, Tamiya, Yamasaki, arXiv:2402.09606 3

Obstacle: Overheads of FTQC n #physical qubits [[n, k, d]]Two conventional approaches for FTQC to achieve $p_0 < p_{\rm th} \Rightarrow p_L \lessapprox \frac{\epsilon}{WD}$ #logical gubits d distance <u>1: Quantum low-density parity-check (LDPC) code</u> 2: Concatenated code [[7, 1, 3]]7-qubit code $[[n, 1, d = \sqrt{n}]]$ surface code Single logical qubit d: distance L: concatenation level Physical qubit Increase concatenation level L Increase **distance d** $n = 7^L, \ p_L \lessapprox \left(\frac{p_0}{p_{\rm th}}\right)^{2^L}$ $n = d^2, \ p_L \lessapprox \left(\frac{p_0}{n_{\rm th}}\right)^d$ **Obstacle in realizing FTQC**: Polylog overhead → diverging to infinity on large scales Space $\frac{W_{\rm FT}}{W} \approx \operatorname{polylog}\left(\frac{WD}{\epsilon}\right)$ Time $\frac{D_{\rm FT}}{D} \approx \operatorname{polylog}\left(\frac{WD}{\epsilon}\right)$ Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024), Yoshida, Tamiya, Yamasaki, <u>arXiv:2402.09606</u> 4

Summary of Main Results

Results: Concatenation of Q Hamming codes achieves **constant-space-overhead FTQC**

+ We construct an optimized protocol with good performance in practical regimes



Merits: Full protocol + Saving qubits + High threshold 2.4% under circuit noise + Modularity

Yamasaki, Koashi, arXiv:2207.08826 (Nat. Phy. 2024), Yoshida, Tamiya, Yamasaki, arXiv:2402.09606 5

Concatenation of Quantum Hamming Codes



Concatenating quantum Hamming codes at growing rate yields a non-vanishing overall rate

Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024)

Efficient Decoder



• Syndrome bitstring = the **binary representation** of the location of a single error

• Extraction of high-weight syndrome by Knill or Steane QEC, applicable to concatenated code

Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024)

Error Correction for Concatenated Codes



Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024)

Full Construction of Fault-Tolerant Protocol

For I=L,L-1,...,1,





Level-I circuit

$ \overline{0} angle$ —/ EC \overline{X}^{i_1} EC –	$\overline{R_y(\pi/4)}$ EC	EC	$C - \overline{H} - EC - \overline{Z} =$
$ \overline{0}\rangle$ —/ EC \overline{X}^{i_2} EC –	$\overline{R_y(\pi/4)}$ EC \overline{Z}		$C - \overline{H} - EC - \overline{Z} - \overline{Z}$
$ \overline{0} angle$ —/ EC \overline{X}^{i_3} EC –	$\overline{R_y(\pi/4)}$ EC \bullet	$-EC - \overline{Z} - E$	$C \longrightarrow \overline{H} \longrightarrow EC \longrightarrow \overline{Z}$
$ \overline{0} angle$ —/ EC \overline{X}^{i_4} EC –	$\overline{R_y(\pi/4)}$ EC \overline{Z}		$C \longrightarrow \overline{H} \longrightarrow EC \longrightarrow \overline{Z} \longrightarrow$
$ \overline{0} angle$ —/ EC \overline{X}^{i_5} EC –	$R_y(\pi/4)$ EC	$-EC - \overline{\overline{Z}} - E$	$C \longrightarrow \overline{H} \longrightarrow EC \longrightarrow \overline{Z} \longrightarrow$
$ \overline{0} angle$ —/ EC \overline{X}^{i_6} EC –	$\overline{R_y(\pi/4)}$ EC \overline{Z}		$C \longrightarrow \overline{H} \longrightarrow EC \longrightarrow \overline{Z} \longrightarrow$
$ \overline{0} angle$ —/ EC \overline{X}^{i_7} EC –	$\overline{R_y(\pi/4)}$ EC	$-EC - \overline{Z} - E$	$C \longrightarrow \overline{H} \longrightarrow EC \longrightarrow \overline{Z} \longrightarrow$

Level-(I-1) circuit to implement logical level-I circuit

Contribution: Explicit protocol (decoder/gate/compilation) & thorough runtime analysis

- Recursively replace operation with gadget & insert error correction in between
- For quantum Hamming codes, **transversal gates** are logical $H^{\otimes k}$, $CNOT^{\otimes k}$, Pauli
- All the other gates by **gate teleportation** with fault-tolerant preparation of auxiliary states

Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024)

Construction of Gadgets for Operations

Fault-tolerant preparation by verification Transversal operations ____/ level-l_register_ /level-l register $Z_{K^{(l)}}$ Measurement $|0\rangle^{\otimes K^{(l)}}$ Initial state ____/ level-l_register_ Pauli /level-l register $\bigotimes_{k^{(l)}=1}^{K^{(l)}} P_{k^{(l)}}$ ____/ level-l_register_ ____/ level-l_register_ ____/ level-l register_⊗ $\left|\Phi^{(0)}\right\rangle \propto (\left|00\right\rangle + \left|11\right\rangle)^{\otimes 2}$ Clifford ____/level-l_register_ Hadamard /level-l register $H^{\otimes K^{(l)}}$ ____/ level-l_register_ U_C : Two-register Clifford ____/level-l_register_ level-*l* register CNOT /level-l register $\mathbf{Y} \otimes K^{(l)}$ ____/ level-l_register_ ____/ level-l_register level-l register /level-l register 4 CZ $R_y(\theta) = \begin{pmatrix} \cos(\theta) & -\sin(\theta) \\ \sin(\theta) & \cos(\theta) \end{pmatrix}$ Non-Clifford /level-l register $Z \otimes K^{(l)}$ _/level-l register /level-l register _ _ _ / level-l register_ Wait _ _ _ / level-l register /level-l register ____/level-l_register_

Explicit construction of a full set of gadgets for all operations required for FTQC

Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024)

Gates by Gate Teleportation



Universal gate set implemented by gate teleportation using fault-tolerant state preparation

Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024)

Provable Existence of Threshold

Error model: Local stochastic error model

s different locations in a circuit of physical qubits may become faulty with probability $< p_0^s$



We can show by induction for I=1,2,3...

Level-(I-1) circuit to implement logical level-I circuit

with increasing parameter of

quantum Hamming codes linearly

$$[[n_l = 2^r - 1, 2^r - 1 - 2r, 3]], r = l + 3$$

Size of ExRec:

- Logical level-l circuit undergoes the local stochastic error model growing polynomially in the code size
- The logical error rate of the level-I circuit is $p_l \leq \left(\frac{\text{poly}(n_l)}{2}\right) p_{l-1}^2 \leq 2^{\alpha l} p_{l-1}^2, \ (\alpha > 0)$

Maximum probability of having two errors in each ExRec

Overall logical error rate: the same bound as conventional concatenated codes

$$p_{L} \leq 2^{\alpha L} p_{L-1}^{2} \leq 2^{\alpha (L2^{0} + (L-1)2^{1})} p_{L-2}^{2^{2}} \leq \dots \leq 2^{\alpha (L2^{0} + (L-1)2^{1} + \dots + 12^{L})} p_{0}^{2^{L}} = O\left(\left(\frac{p_{0}}{p_{\text{th}}}\right)^{2^{L}}\right)$$

Geometric sequence

Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024)

Requirements for Practical FTQC

- Logical gates
- Low space overhead Covered by Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024)
- Short time overhead
- High threshold
- Modular implementation

Problem

- Conventional protocols require large space overhead
- High-rate QLDPC codes sacrifice time, threshold, and modularity

→ Our new optimized protocol takes care of all essential requirements Yoshida, Tamiya, Yamasaki, <u>arXiv:2402.09606</u>

Yamasaki, Koashi, <u>arXiv:2207.08826</u> (Nat. Phy. 2024), Yoshida, Tamiya, Yamasaki, <u>arXiv:2402.09606</u> 13

Underlying Codes to Improve Threshold



Yoshida, Tamiya, Yamasaki, <u>arXiv:2402.09606</u>

90-97% saving of space overhead

- Threshold of the original protocol based on quantum Hamming codes: 10⁻⁵
- Logical error rate of C4/C6 code < 10⁻⁷

with a few hundred physical qubits

- C4/C6 protocol has threshold 2.4%
- Start with C4/C6 code (Next slide) Knill, arXiv:quant-ph/0410199, Nature (2005)
- Switch to quantum Hamming codes $[[15,7,3]], [[31,21,3]], [[63,51,3]], \dots$ High-rate
 - →Achieving constant space overhead

C4/C6 Code

Merit: Threshold for protocol based on C4/C6 code : 2.4% vs Threshold for surface code: 0.3%



Protocol

8 qubits in 1D periodic arrangement

6 level-1 registers in 1D periodic arrangement







Preparation of [[6, 2, 2]] code

Preparation of [[4, 2, 2]] code

Knill, arXiv:quant-ph/0410199 (Nature 2005)

Threshold Analysis

		Spa	ce overhead	
	Threshold	p=0.01 $%$	p=0.1%	p=1%
C_4/C_6 code	2.4%	18	54	1458
Surface code	0.31%	121	841	-
Steane code	0.030%	343	-	-
C_4/S teane code	0.15%	14	4802	-

Our paper includes...

/level-l register level-(l-1) register level-(l-1) register $|+\rangle$ level-(l-1) register $|0\rangle$ $-\dot{X}$ X / level-(l-1) register $|+\rangle$ -Xlevel-(l-1) register $|0\rangle$ Xlevel-(l-1) register $|0\rangle$ -XXlevel - (l-1) register $|0\rangle$ /auxiliary level-(l-1) register $|0\rangle$ |X|/level-l register level-(l-1) register level-(l-1) register /level-(l-1) register level-(l-1) register level-(l-1) register level-(l-1) register X \overline{X} Comparison of level-(l-1) register level-(l-1) regi preparations of level-(l-1) registe $-\dot{X}$ $|0\rangle$ level-(l-1) register evel-(l-1) register $|0\rangle$ +X \overline{X} Steane code level-(l-1) register $|0\rangle - X$ auxiliary level-(l-1) register $|0\rangle$

Yoshida, Tamiya, Yamasaki, <u>arXiv:2402.09606</u>

Our contribution: Systematic comparison

- Under circuit-level depolarizing noise
- Threshold for CNOT gate (not memory)
- Hard-decision decoder & MWPM decoder

Numerical simulation in the same setting



Modularity

Litinski, arXiv:1808.02892

Error suppression by concatenated Q Hamming codes:

Could this controllably scale up?



Logical error rate: Decaying much faster

More flexibility in architecture design on large scales

Challenge: Full control of a large LDPC-code chip

Solution: Concatenation = Abstraction



Unit at lower error rate

Concatenate the units to scale up

Opening a way of low-overhead FTQC by concatenating small-size modular parts

Yamasaki, Koashi, arXiv:2207.08826 (Nat. Phy. 2024), Yoshida, Tamiya, Yamasaki, arXiv:2402.09606 17

New criteria for physical implementation of quantum computation

Design principle: Finite technological requirement + Threshold behavior + Modularity



Develop finite-size fault-tolerant modules Let the modules be equipped with communication interfaces **Goal** : Abstract modules by QEC+Inferfaces for scaling up Combine finite-size modules by interfaces to make a concatenated code Form a higher-level module at low error rate from lower-level modules Repeat this procedure to suppress error rate, so we have more margin

H. Yamasaki, S. Sunami, A. Goban, in preparation

Conclusion

Results: Concatenation of Q Hamming codes achieves **constant-space-overhead FTQC**

+ We construct an optimized protocol with good performance in practical regimes



We did not improve a protocol What we need was a new approach

Merits: Full protocol + Saving qubits + High threshold 2.4% under circuit noise + Modularity

 \rightarrow Concatenate codes, save qubits

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Yamasaki, Koashi, arXiv:2207.08826 (Nat. Phy. 2024), Yoshida, Tamiya, Yamasaki, arXiv:2402.09606 19