Title: Wideband digital signal processing for EHT & SMA

Date: Nov 14, 2014 12:00 PM

URL: http://pirsa.org/14110122

Abstract: To improve the EHTâ€™s sensitivity, resolution and imaging fidelity one might enhance station collecting area, add stations, or increase bandwidth. The latter improvement, bandwidth, is probably the most accessible. For many stations, including Submillimeter Array (SMA), the bandwidth is limited not by the receiver but by the digital signal processing. This talk will describe digital development at SMA. The upgraded SMA will contribute directly to the EHT, and technology under development has potential to benefit other EHT stations as well.


EXIT

Current SMA specifications

Array

baseline length	8 - 509m
best resolution (230 GHz) (345 GHz) (690 GHz)	 0.4" 0.3" 0.15"
sensitivity (DSB, 6 hours) (230 GHz - 2.0mm H_2O) (345 GHz - 1.5mm H_2O) (690 GHz - 1.0mm H_2O)	 0.6 mJy 1.6 mJy 20. mJy

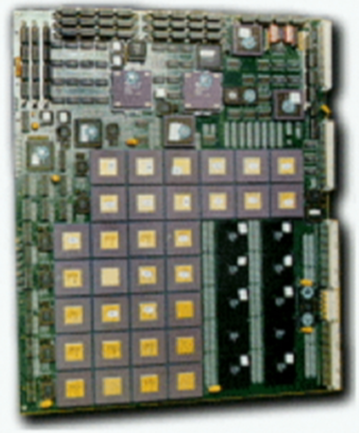
Antennas

quantity	8
diameter	6m
surface accuracy (rms)	12-20μm
aperture efficiency (230 GHz) (345 GHz) (690 GHz)	 0.70-0.80 0.60-0.75 0.40-0.55
pointing accuracy (rms)	~3"
slew rate	4°/s

Mark 4 XF 'CB'
(Canaris ASIC from 1995)

90 CBs in system
32 ASICs/CB = 2880 ASIC/system

~25 kW (digital)+analog+cooling



Receivers

frequency (GHz) wavelength (mm)	230 1.3	345 0.87	690 0.43
primary beam (")	55	36	18
T_{sys} (DSB, K)	80-200	150-350	800-4000

IF/Backend

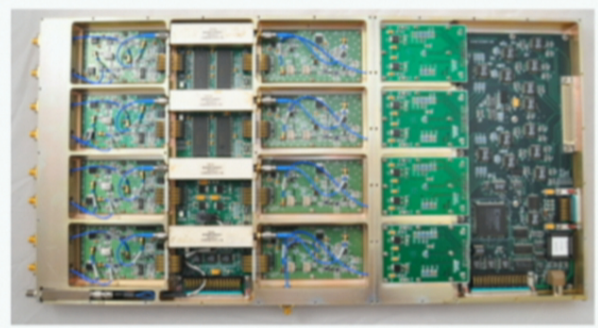
bandwidth	1.968 GHz
spectral resolution (single rx) max (uniform over full 2GHz) max (without bandwidth loss) max (true limit)	 0.406 MHz 0.203 MHz 0.025 MHz
data format	MIR (OVRO)

DSP: ASIC-based, highly parallel

IF downconverter and sampler assembly (C2DC)

8 antennas x 6 'blocks' x 2 pols = 96 assemblies

96 x 4 chunks/block
= 384 IF channels and ADCs

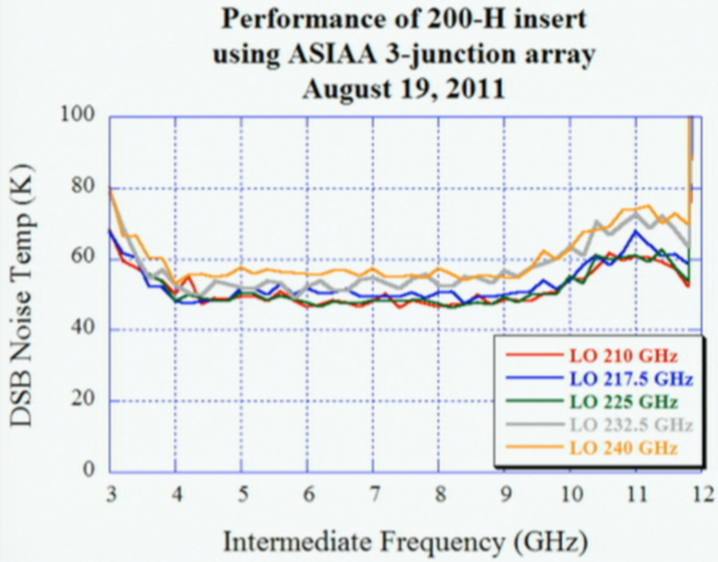


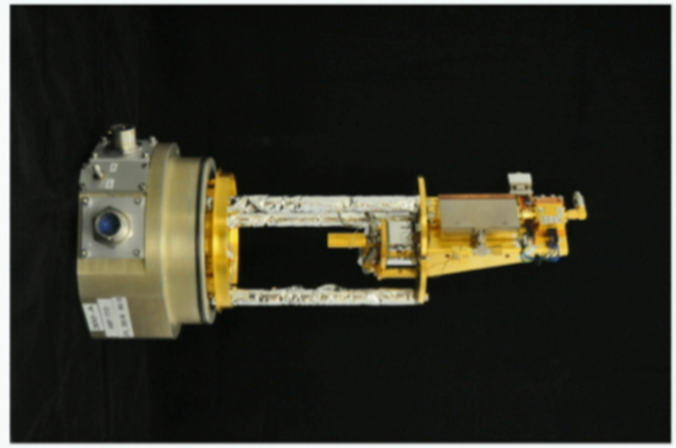
current ASIC correlator is an XF architecture. Modern DSP technology (many wide multipliers on an FPGA) *strongly* favor FX, especially for high f-resolution.

Highly hybridized, 4 GHz band divided into 48 'chunks' per antenna

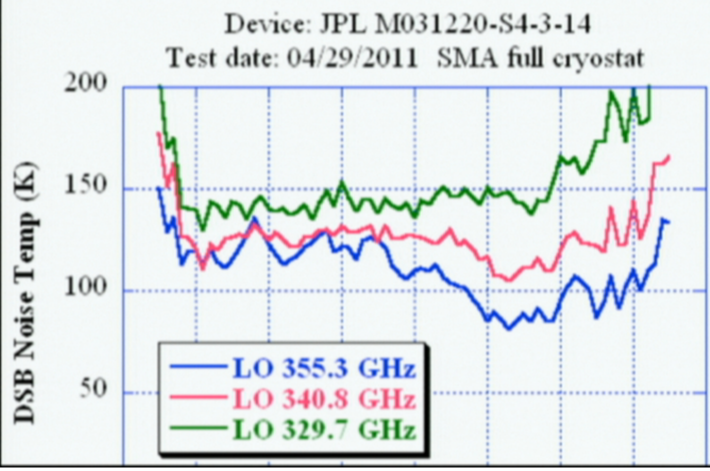
Wideband SIS junction receivers, Tong et al.

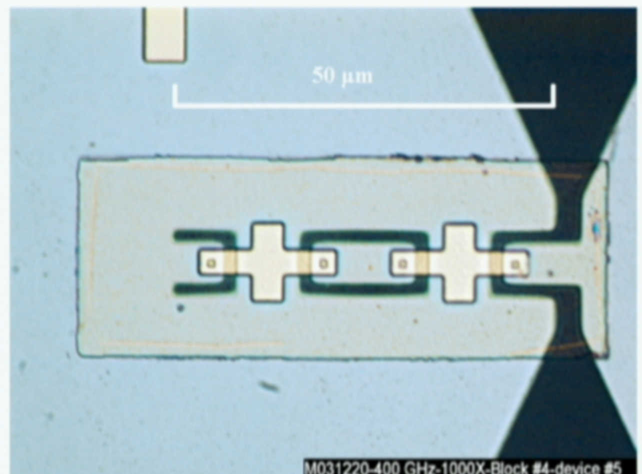
IF amplifiers from Weinreb





SMA receiver insert to demonstrate 300 GHz





400 GHz 4-junction series SIS array

CASPER glossary

•CASPER: Collaboration for Astronomy Signal Processing and Electronics Research
http://casper.berkeley.edu

•ROACH: Reconfigurable Open Architecture Computing Hardware.

•MSSGE: Matlab-Simulink-System-Generator-EDK toolflow

•BORPH: Variant of Linux, controls hardware processes

CASPER glossary

- CASPER: Collaboration for Astronomy Signal Processing and Electronics Research http://casper.berkeley.edu
- ROACH: Reconfigurable Open Architecture Computing Hardware.
- MSSGE: Matlab-Simulink-System-Generator-EDK toolflow
- BORPH: Variant of Linux, controls hardware processes

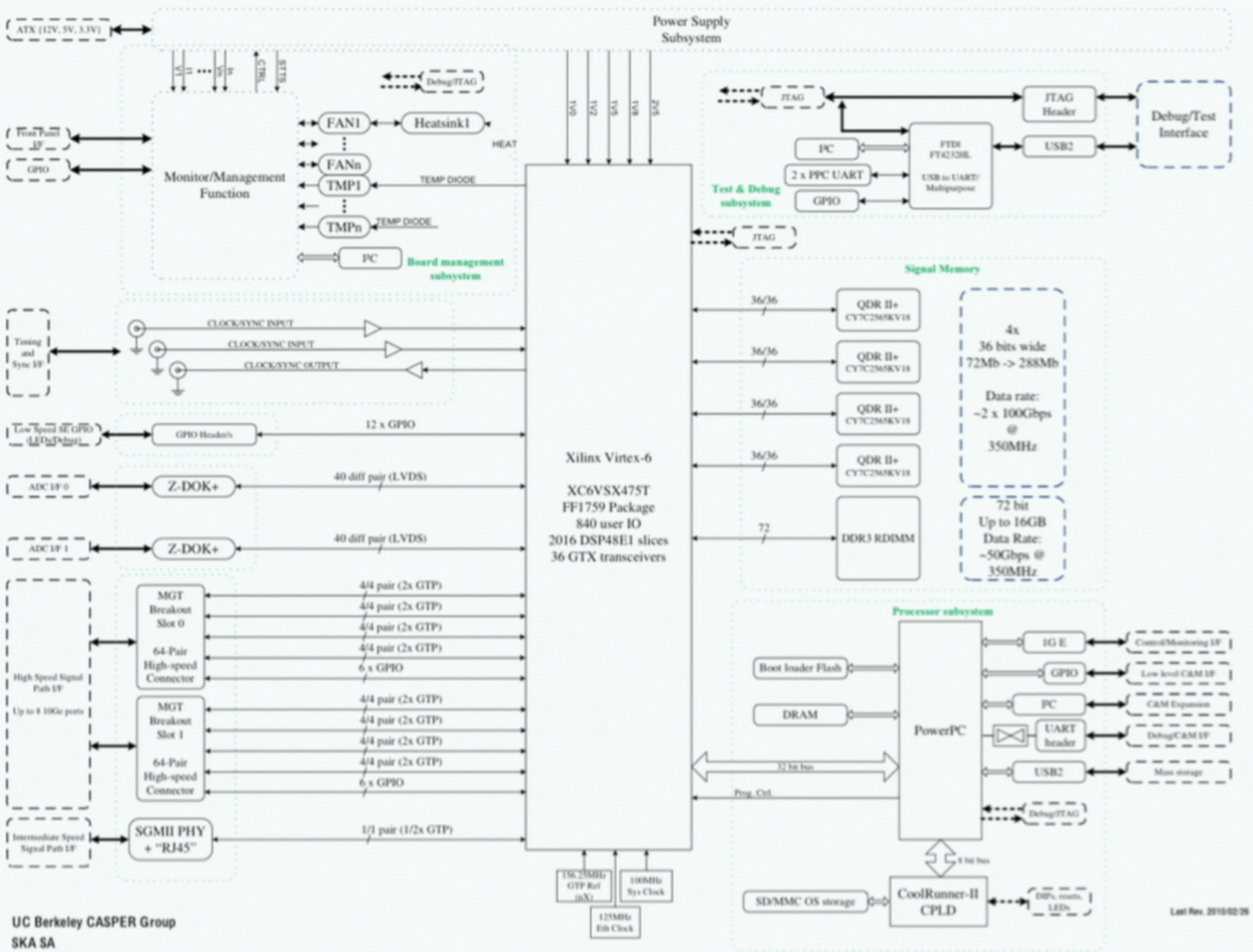
CASPER glossary

- CASPER: Collaboration for Astronomy Signal Processing and Electronics Research
http://casper.berkeley.edu
- ROACH: Reconfigurable Open Architecture Computing Hardware.
- MSSGE: Matlab-Simulink-System-Generator-EDK toolflow
- BORPH: Variant of Linux, controls hardware processes
- ROACH Motel, custom 1U open source enclosure

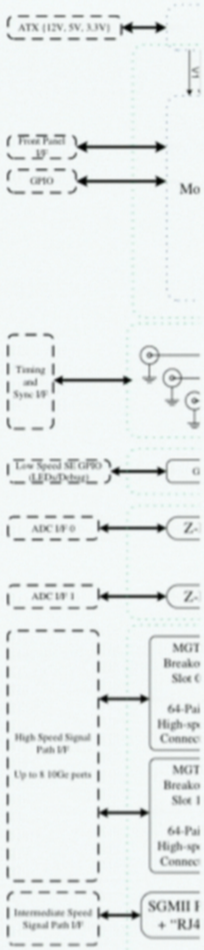
Also:

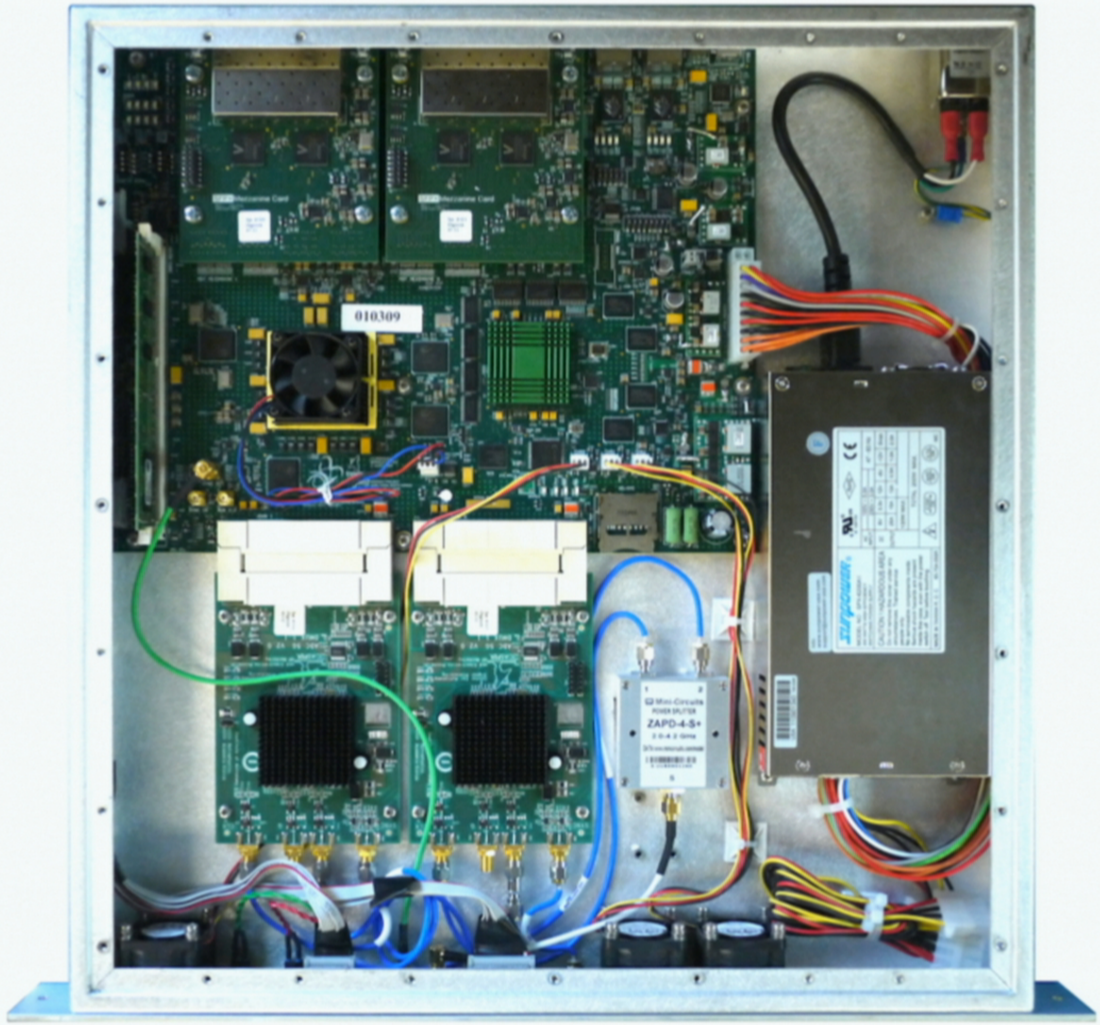
- Variety of ADCs (wide band or many low rate channels)
- Simulink libraries of high level functions, many for astronomy
- GPU methods

ROACH 2 based on Xilinx Virtex 6 SX475T



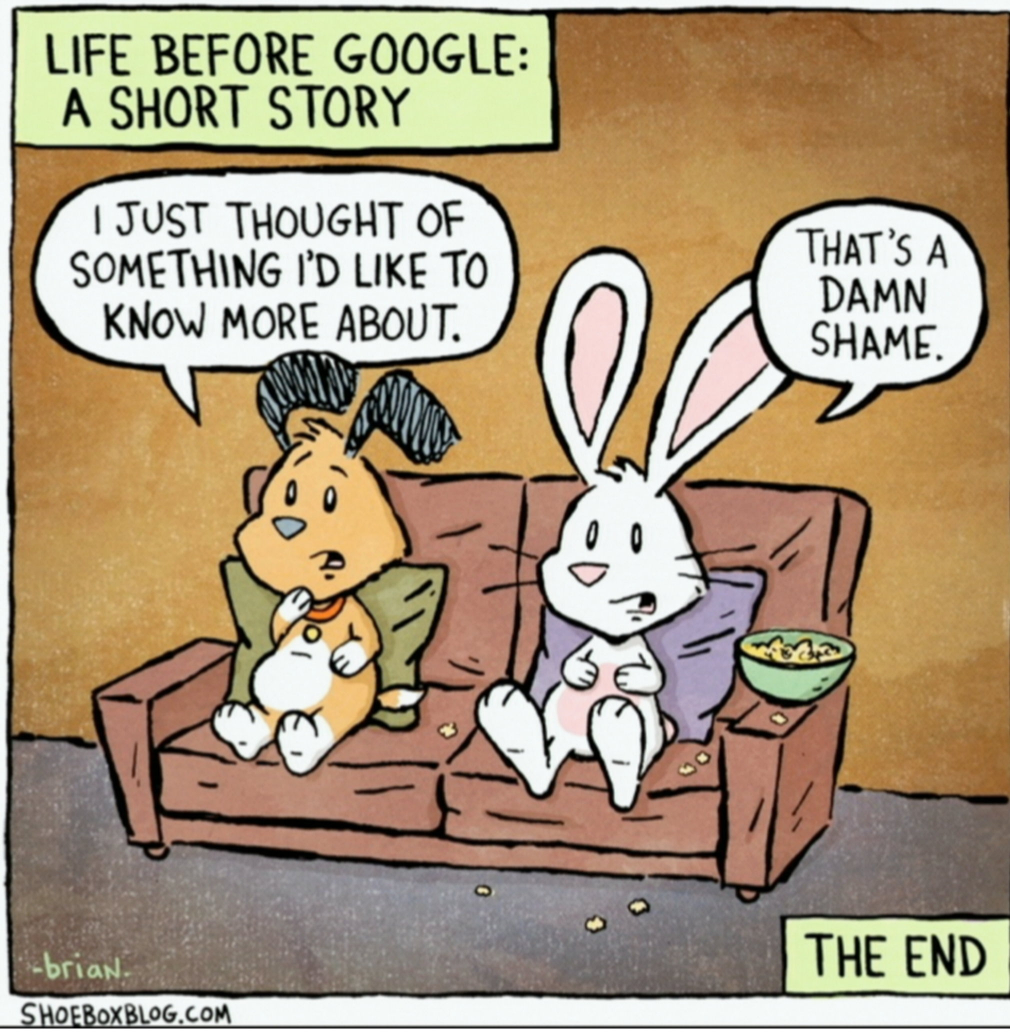
ROACH 2 based on Xilinx Virtex 6 SX475T





UC Berkeley CASPER Group
SKA SA

Ultra Fast Analog to Digital Converters

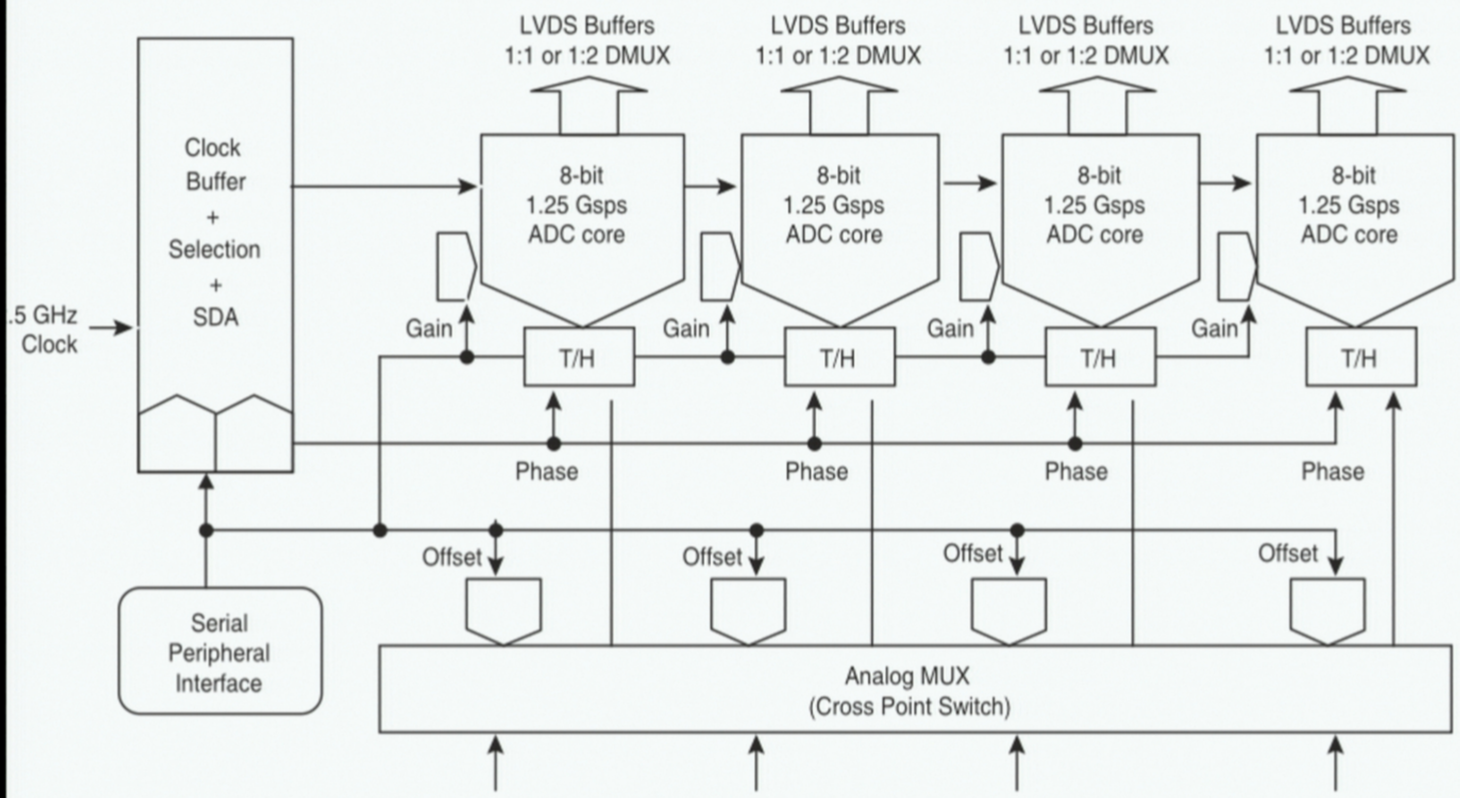


Ultra Fast Analog to Digital Converters

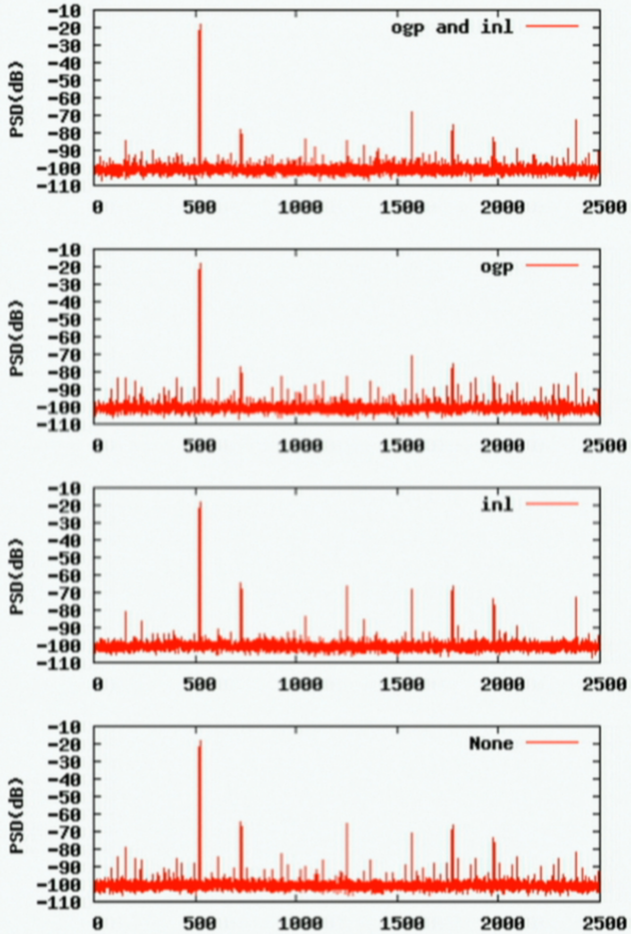
f_s(GSa/s)	BW (GHz)	# bits	Manuf.	Part #	~cost	remarks
5	2.0	8	e2v	EV8AQ160	$300	ASIAA board H. Jiang
10	20	4	Adsantec	ASNT7120-KMA	$800	3.5 ENOB, 2W
12.5	8	8	Maxtek	—	$17k	mature module
20	8	5	e2v	EV5AS210	$7k	Torres et al., IRAM
20	13	8	Agilent	—	—	
20	10	3+over	Hittite	HMC5401LC5	$2k	eval board $7k
30	14	6	Micram	ADC30	$10k	only demo 12 GSa/s
40	13	68	Guzik	WDM5121	—	snapshot, 4 Gpt memory
56	15	8	Fujitsu	CHAIS	—	snapshot, no stream
20	10	1	Hittite	HMC874LC3C	$40	clocked comp, no demux
12.5	14	1	Inphi	1385DX	—	latched comp, 1:8 demux
25	18	1	Inphi	25707CP	—	latched comp, no demux

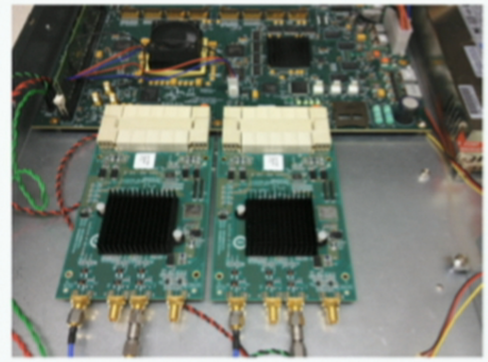
- A faster sampler translates to simpler analog IF system, legacy SMA 208 MHz
- present 4 GHz 8-antenna SMA IF/LO has 384x82 MHz chunks lots of $, time
- 4 GHz BW (2 GHz DP), 2 GHz blocks: 16 chunks (now)
- 16 GHz BW (8 GHz DP) 2 GHz blocks: 64 chunks (SMA/EHT Goal)
- 16 GHz (8 GHz DP) 8 GHz blocks: 16 chunks (needs ~20 GS/s ADC)

EV8AQ160: 5 GS/s quad cores interleaved

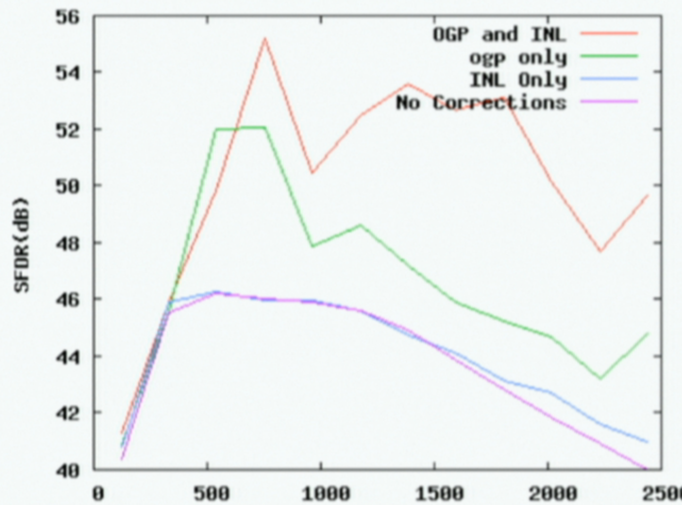


5 GS/s quad core artifacts



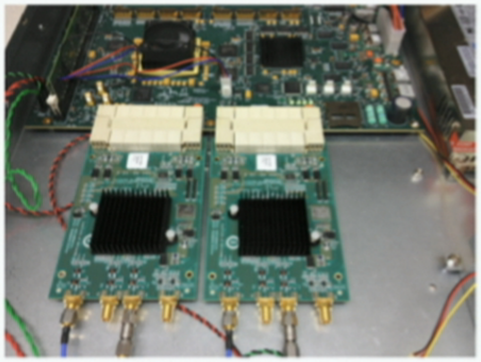


Spurious free dynamic range

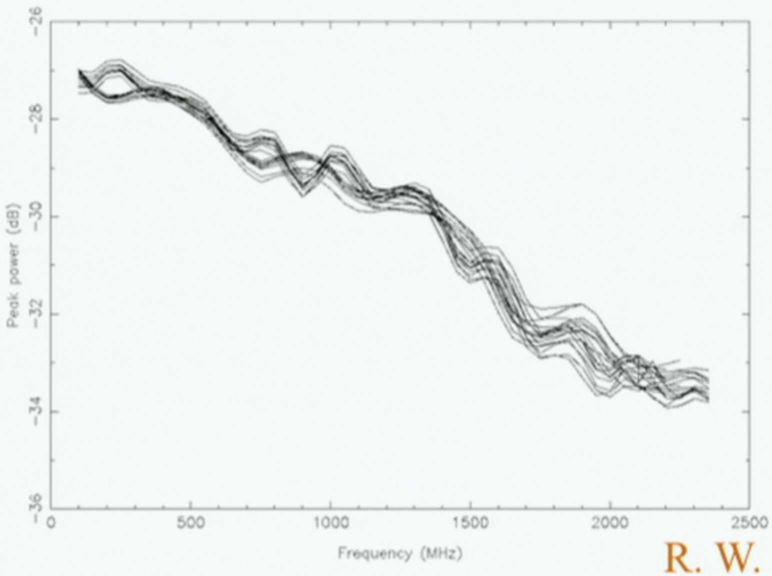


Patel, Wilson, et al, J. Astron. Instrum., 03, 2014

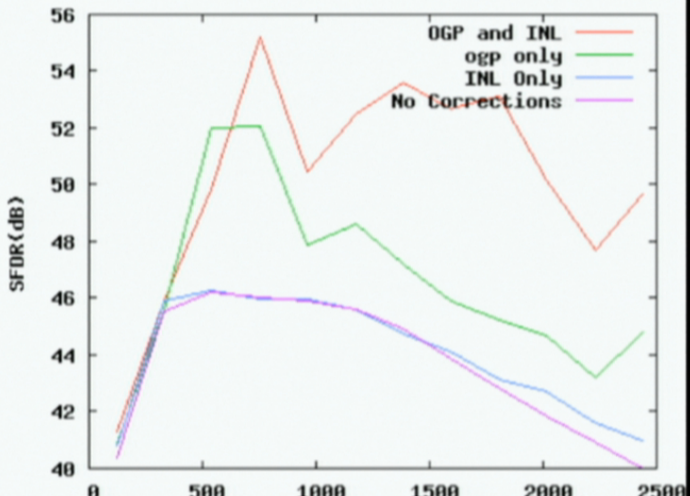
5 GS/s quad core artifacts



Frequency response (19 ADCs)

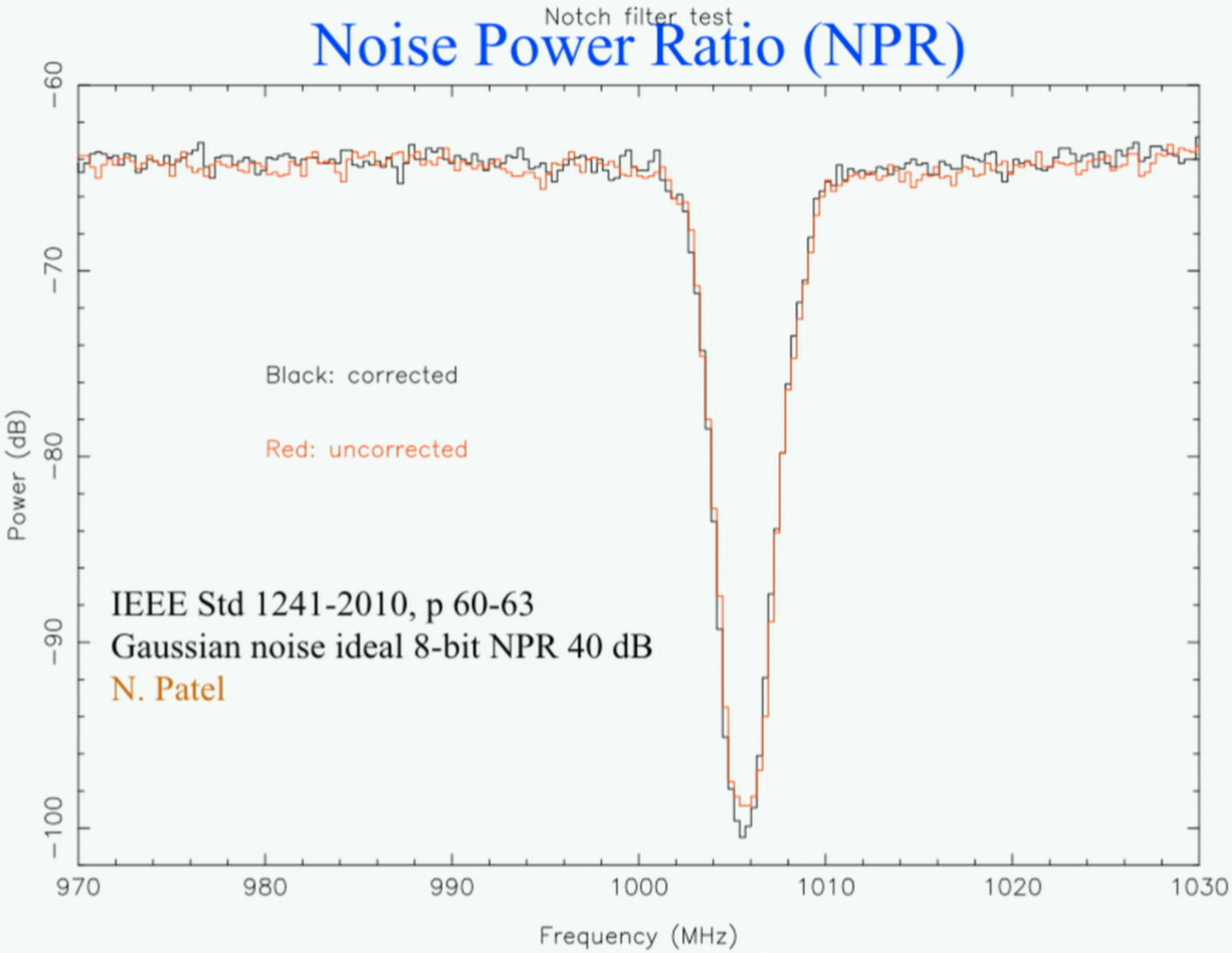


Spurious free dynamic range



R. W. Wilson

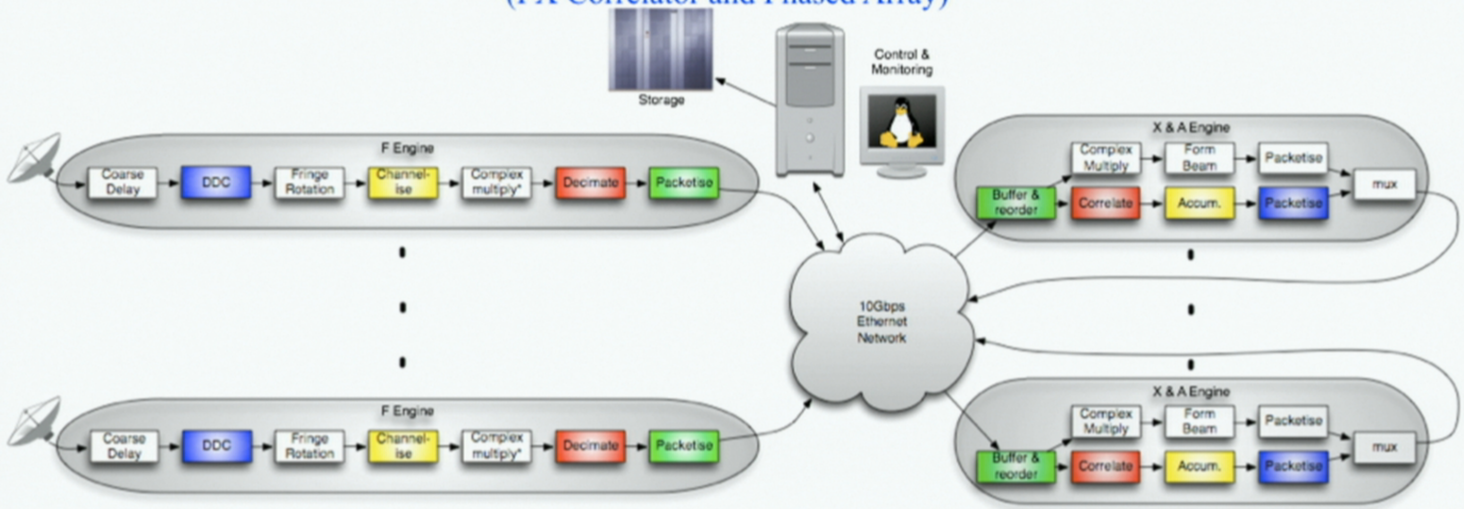
Noise Power Ratio (NPR)



IEEE Std 1241-2010, p 60-63
Gaussian noise ideal 8-bit NPR 40 dB
N. Patel

CASPER Packetized Back End

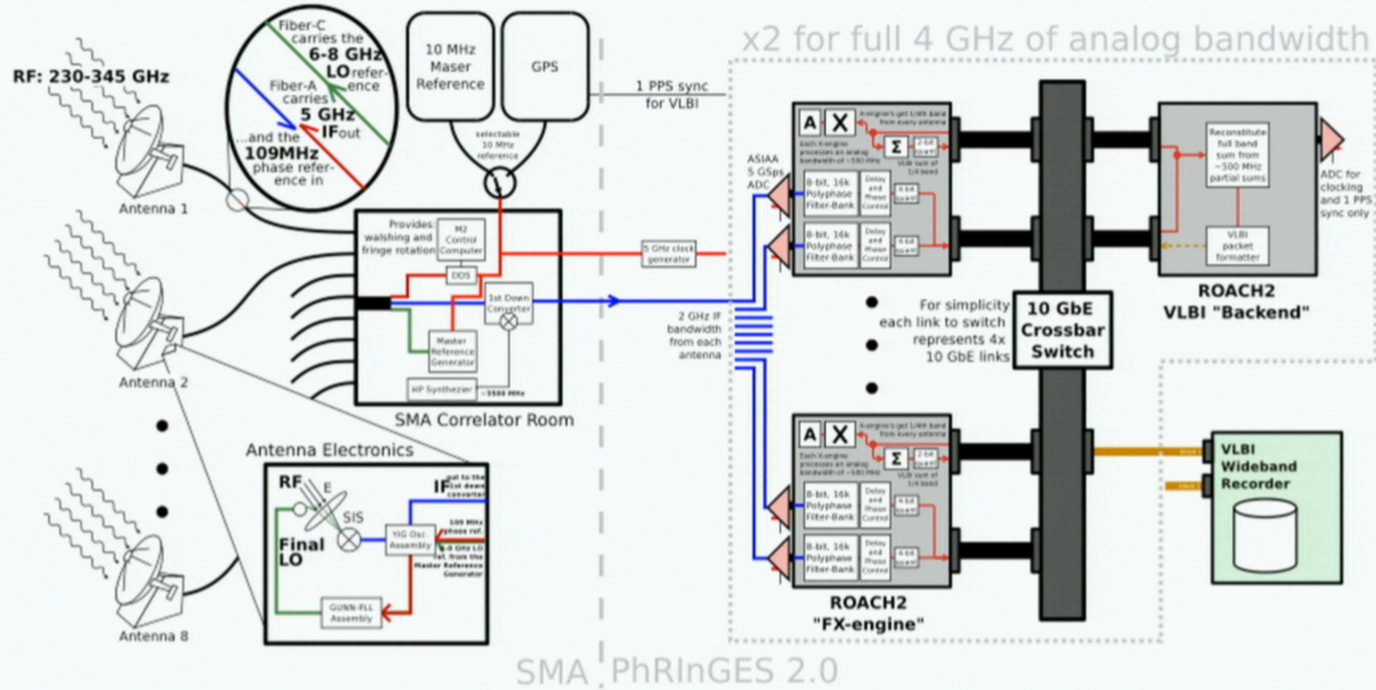
(FX Correlator and Phased Array)



*Complex multiply allows for fine delay control and per-channel digital gain control.
White coloured blocks not yet implemented.

- 2 x 4.6 GS/s 8-bit ADC per ROACH2; 2.3 GHz Nyquist band, 2 F-engines per R2
- truncated to 4 bits at channelized 10GigE output: 2 x 4.6 x 4 = 37 Gb/s
- One ROACH 2 can then handles 4 GHz usable using 4 10GigE ports per ROACH2
- +1 port per ROACH2 for phased sum out, so 5 ports per ROACH2, 40 port switch
- # of F-engines: 2 blocks x 8 antennas x 2 pol = 16
- 2 X-engines / ROACH2 => 8 ROACH2, so combine F-and X-engines on R2

SWARM: SMA Wideband Astronomical ROACH2 Machine



Will be connected to run in parallel with existing correlator, doubling bandwidth. Additional benefits: 1. high spectral res with no sacrifice of bandwidth, 2. smaller footprint for phase-in of SWARM2 etc, 3. native VLBI support over full 4 GHz band, and 4. better correlator efficiency with 8 bit ADC

Feature	Specification	Remarks
Number of antennas	8	2 receivers each.
Bandwidth per receiver	2 GHz	Dual polarization in each side band.
Number of sidebands	2	90-270 Walsh splits SBs, Rx are DSB
Simultaneous receivers	2	Dual frequency or dual polarization 230 & 345 GHz
Baselines	56	28 per Rx, full Stokes, 112 total
Spectral resolution	140 kHz	2.3 GHz Nyquist / 16384 channels
Fastest dump rate	0.65 s	Single full Walsh cycle
Phased array bandwidth	4 GHz	2 GHz ×dual pol.

Virtex-6 FPGA Feature Summary

Table 1: **Virtex-6 FPGA Feature Summary by Device**

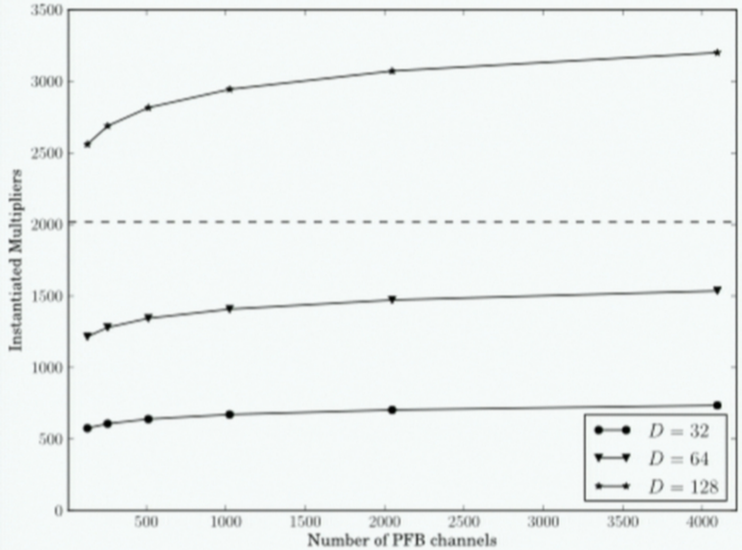
Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks			MMCMs[4]	Interface Blocks for PCI Express	Ethernet MACs[5]	Maximum Transceivers		Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb[3]	36 Kb	Max (Kb)				GTX	GTH		
XC6VLX75T	74,496	11,640	1,045	288	312	156	5,616	6	1	4	12	0	9	360
XC6VLX130T	128,000	20,000	1,740	480	528	264	9,504	10	2	4	20	0	15	600
XC6VLX195T	199,680	31,200	3,040	640	688	344	12,384	10	2	4	20	0	15	600
XC6VLX240T	241,152	37,680	3,650	768	832	416	14,976	12	2	4	24	0	18	720
XC6VLX365T	364,032	56,880	4,130	576	832	416	14,976	12	2	4	24	0	18	720
XC6VLX550T	549,888	85,920	6,200	864	1,264	632	22,752	18	2	4	36	0	30	1200
XC6VLX760	758,784	118,560	8,280	864	1,440	720	25,920	18	0	0	0	0	30	1200
XC6VSX315T	314,880	49,200	5,090	1,344	1,408	704	25,344	12	2	4	24	0	18	720
XC6VSX475T	476,160	74,400	7,640	2,016	2,128	1,064	38,304	18	2	4	36	0	21	840
XC6VHX250T	251,904	39,360	3,040	576	1,008	504	18,144	12	4	4	48	0	8	320
XC6VHX255T	253,440	39,600	3,050	576	1,032	516	18,576	12	2	2	24	24	12	480
XC6VHX380T	382,464	59,760	4,570	864	1,536	768	27,648	18	4	4	48	24	18	720
XC6VHX565T	566,784	88,560	6,370	864	1,824	912	32,832	18	4	4	48	24	18	720

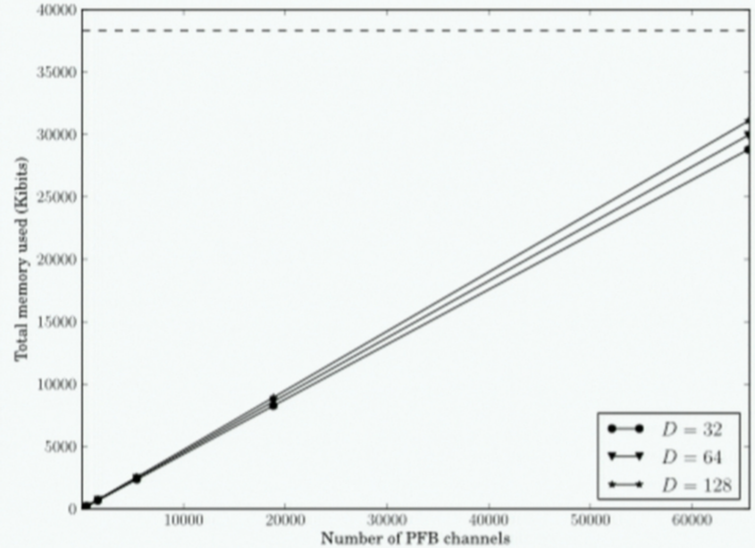
Notes:

1. Each Virtex-6 FPGA slice contains four LUTs and eight flip-flops, only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP48E1 slice contains a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kbits in size. Each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains two mixed-mode clock managers (MMCM).
5. This table lists individual Ethernet MACs per device.
6. Does not include configuration Bank 0.
7. This number does not include GTX or GTH transceivers.

PFB Multiplier, adder and memory utilization in Virtex 6

(Primiani, Weintroub, deWerd, 2011)





$$M_{\mathrm{PFB}} = \underbrace{D \log_2 ND}_{\mathrm{FFT}} + \underbrace{TD}_{\mathrm{FIR}} - \underbrace{2D}_{\mathrm{optimization}}$$

$$A_{\mathrm{PFB}} = \underbrace{\frac{3}{2} D \log_2 ND}_{\mathrm{FFT}} + \underbrace{D(T-1)}_{FIR} + \underbrace{D}_{\mathrm{reorder}}$$

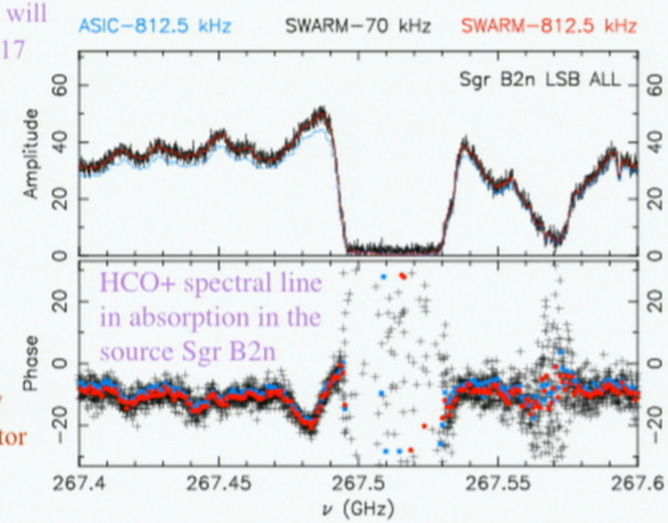
$$R_{\mathrm{PFB}} = b^{\Sigma} N \left(\frac{1}{2} \log_2 D + T + 2 \right) - 5 b^{\Sigma} D$$

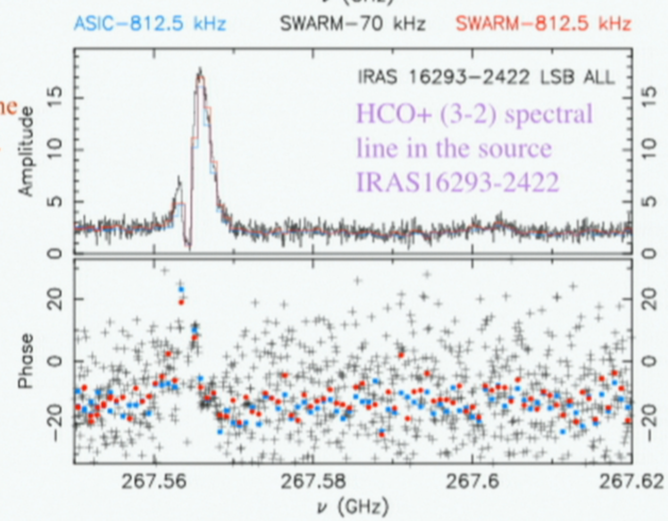
First quadrant SWARM installation at SMA

"SWARM=SMA Wideband Astronomical ROACH2 Machine"

SWARM will be commissioned for science this week. Phased array features will enable 8 Gb/s EHT VLBI in March 2015, 32 Gb/s in 2016, and 64 Gb/s in 2017

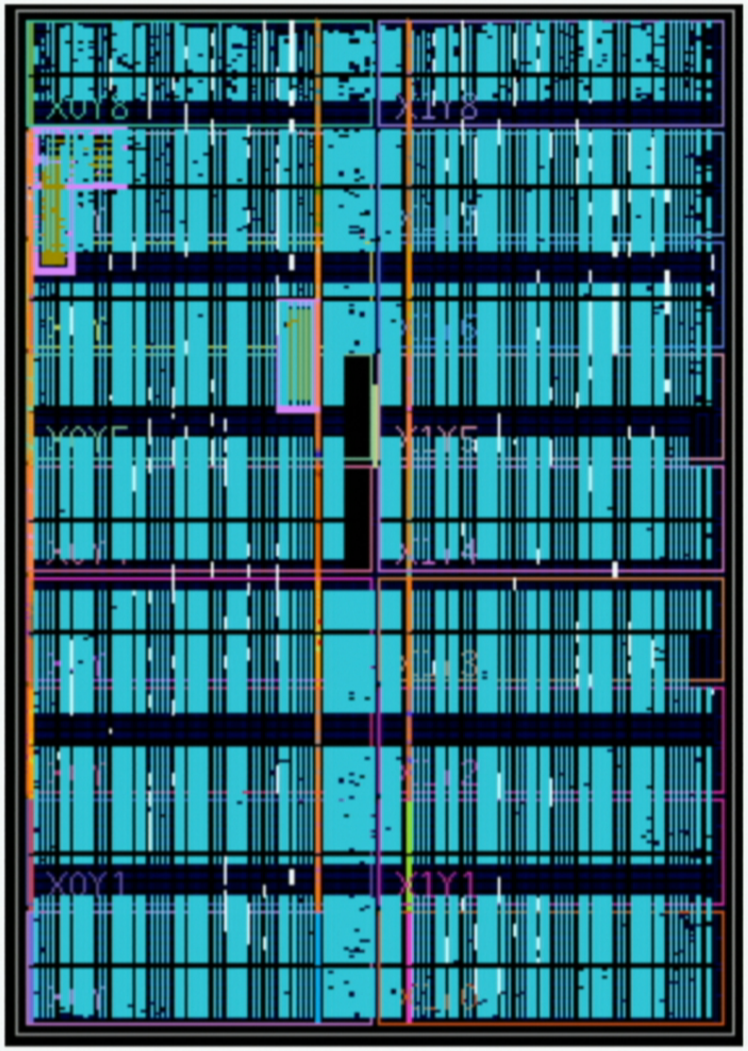
Right: SWARM spectra at 70 kHz resolution in black compared to legacy SMA ASIC correlator data at 812.5 kHz resolution in blue. Red plots show SWARM vector averaged to the same resolution as ASIC.





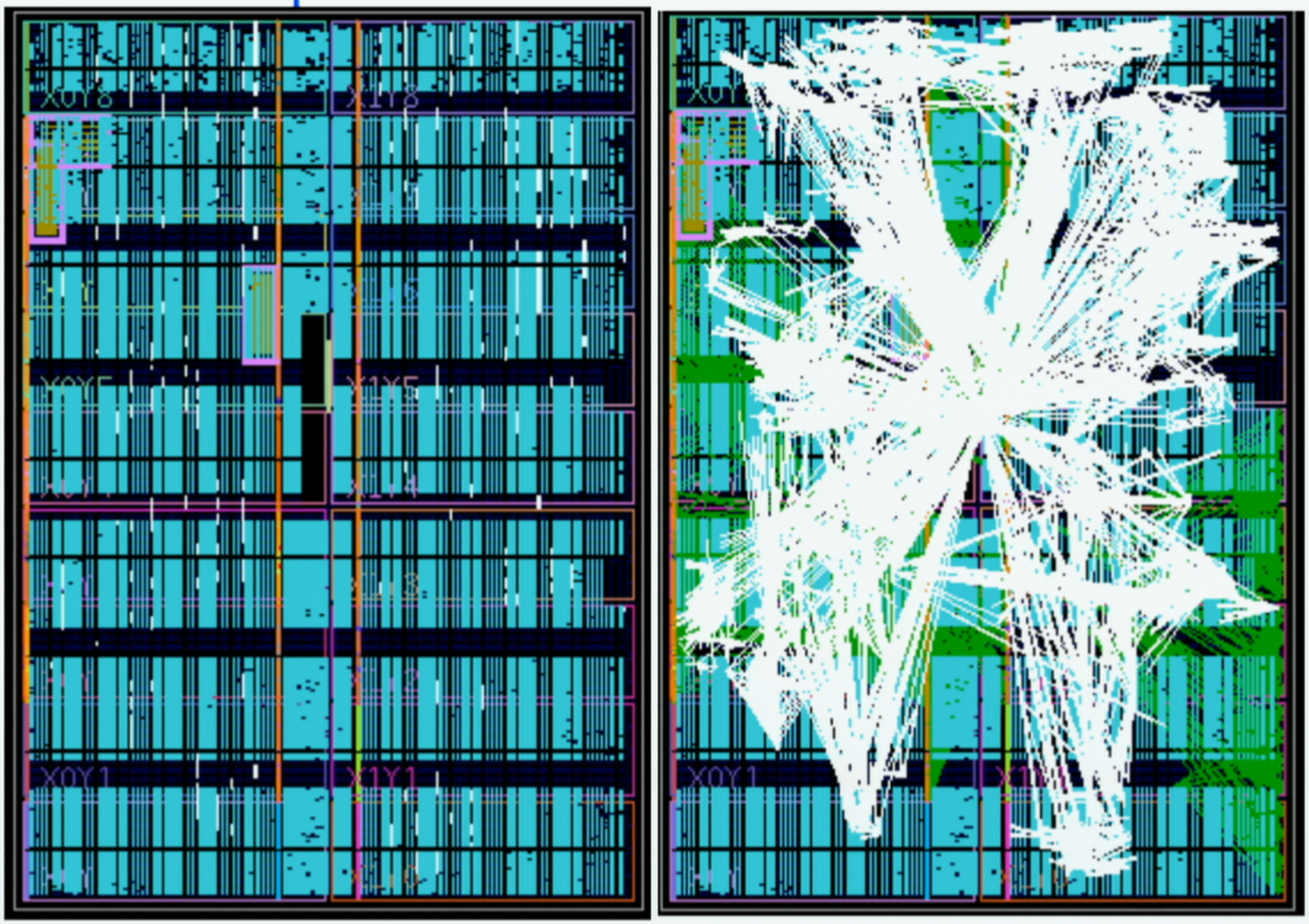
- 8% of the rack space and 5% of the power of ASIC correlator
- additional space and power savings in IF, cooling
- Same bandwidth, substantially enhanced spectral resolution
- VLBI Phased Array capability over the full bandwidth.

Increasing clock speed of FPGA: planAhead

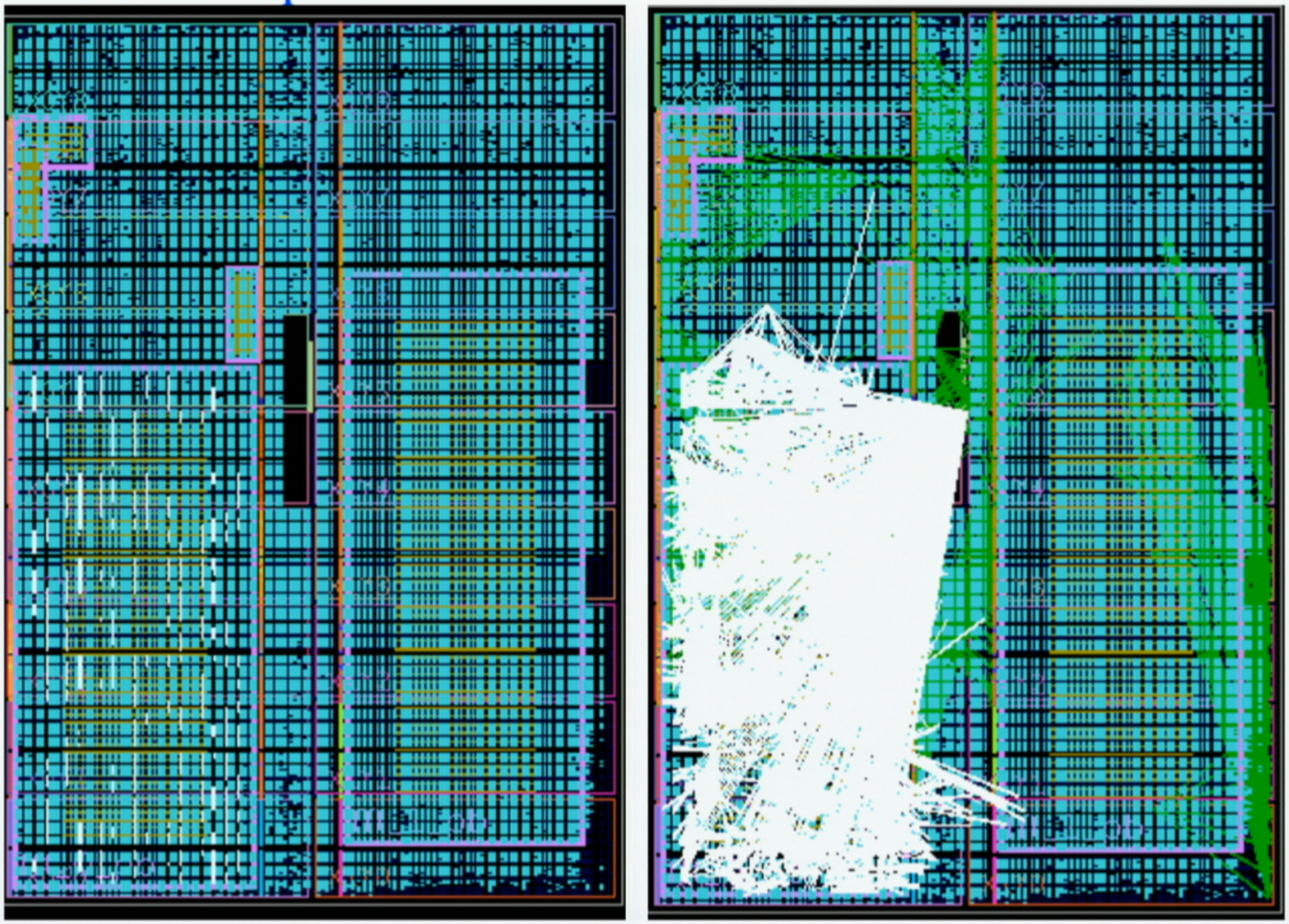


FFT1 Block Memory and DSP48 shown
FFT2 similarly distributed

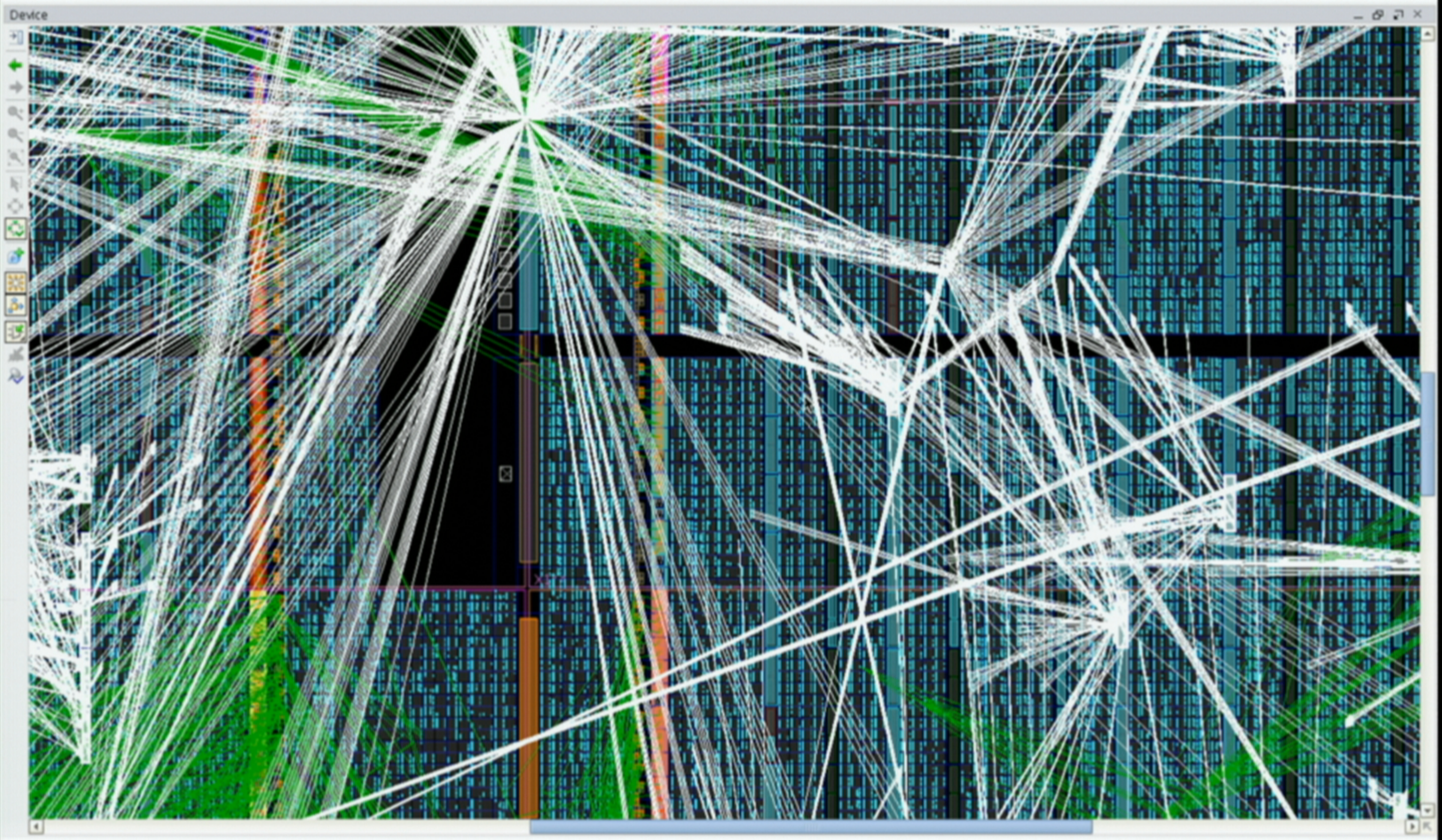
Implementation: “MAP and PAR”



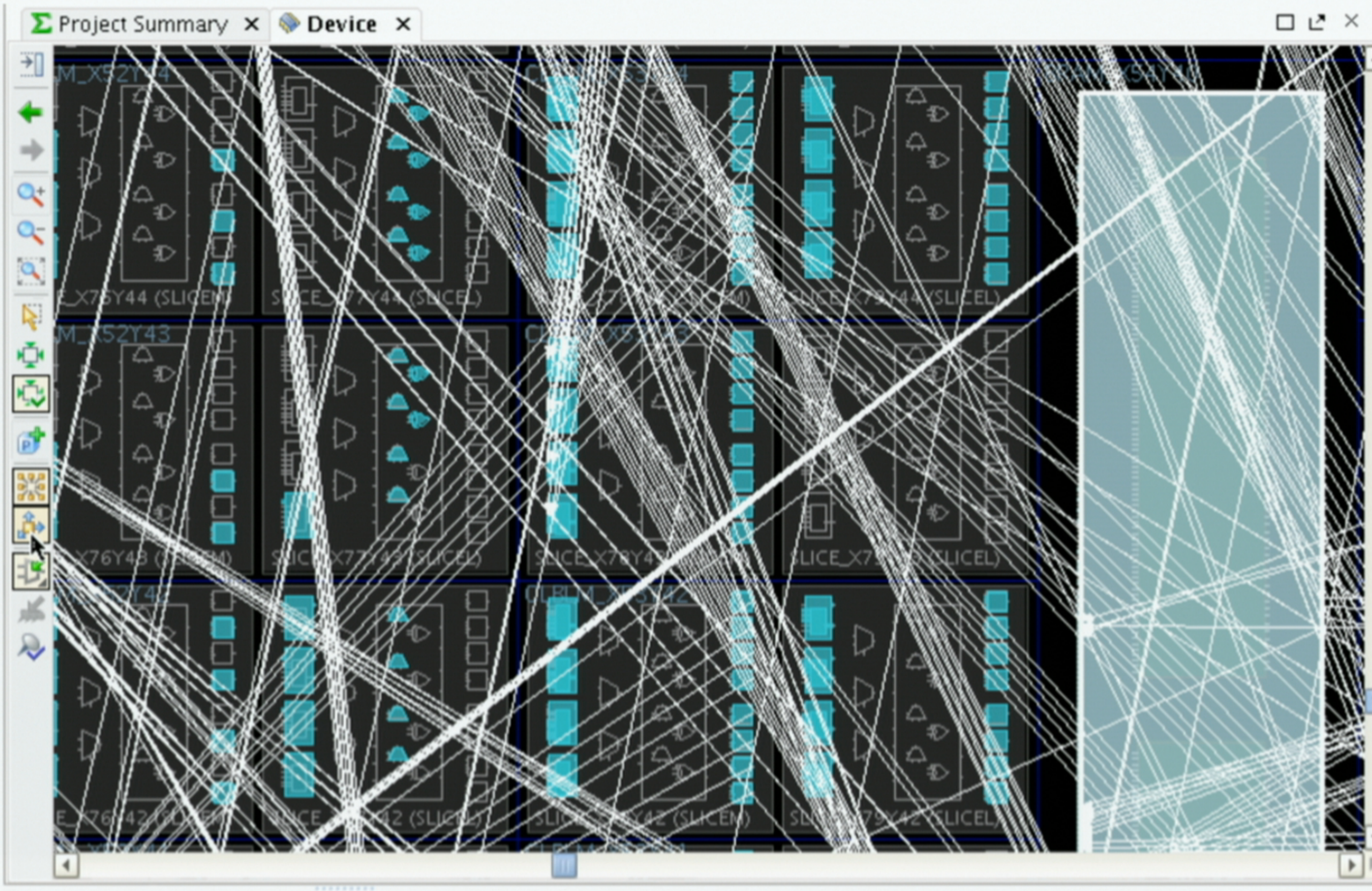
Implementation: “MAP and PAR”



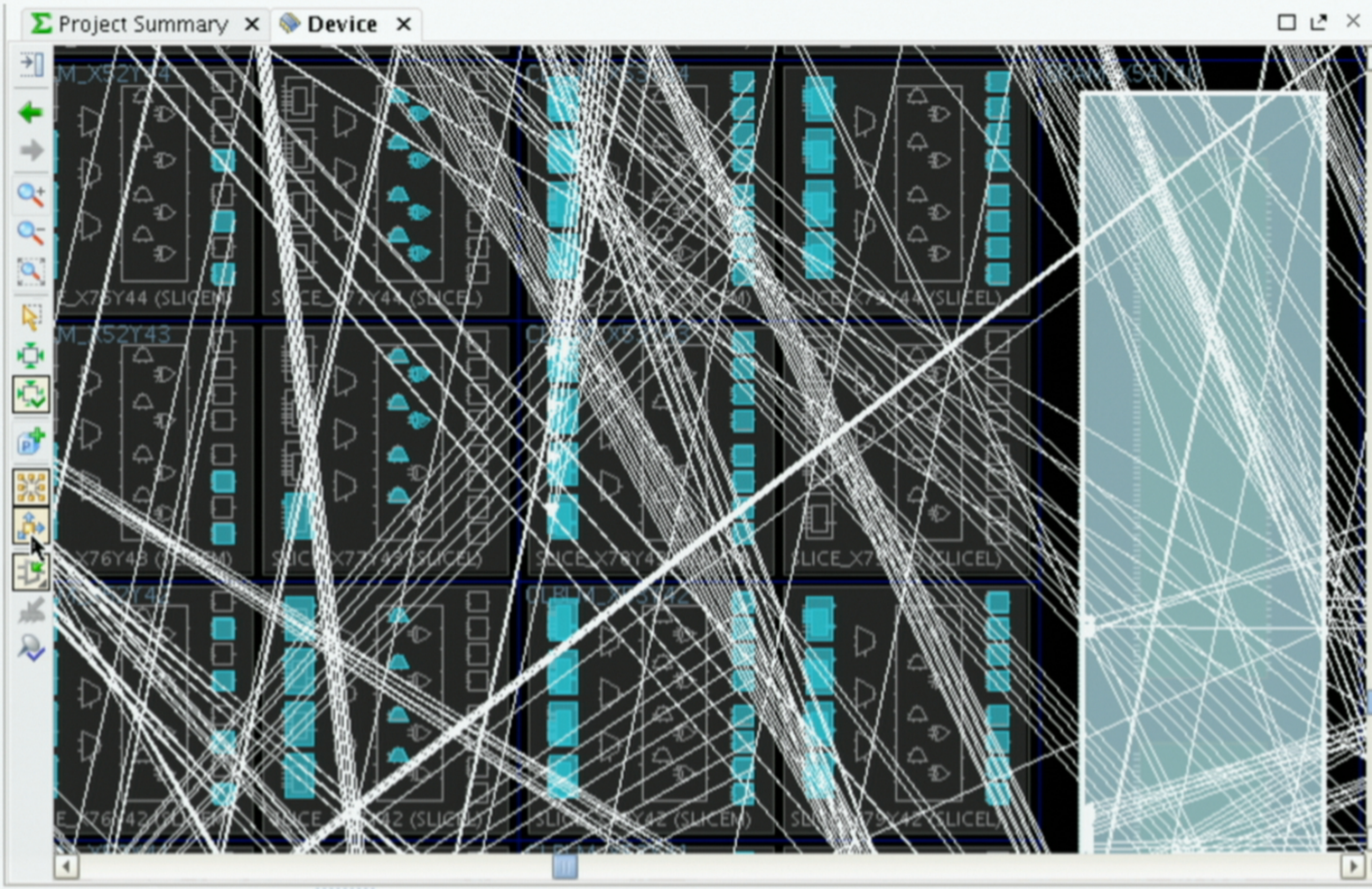
Zoomed view I



zoomed view II

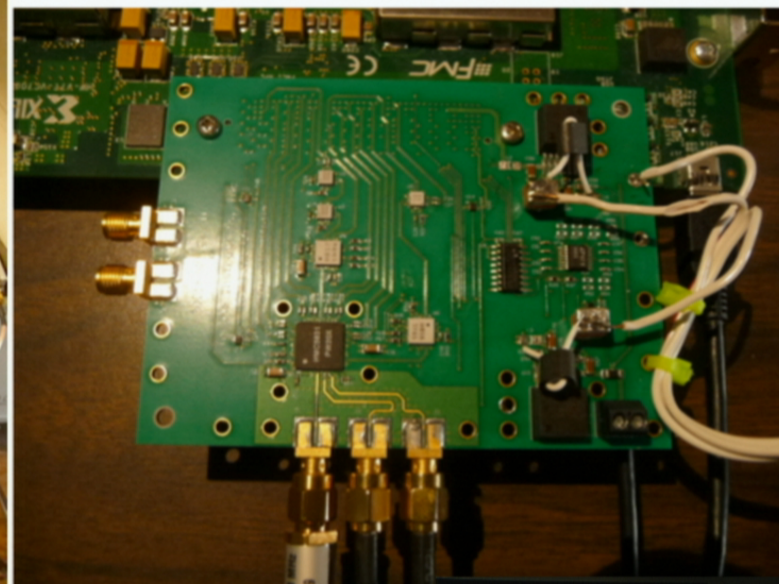


zoomed view II



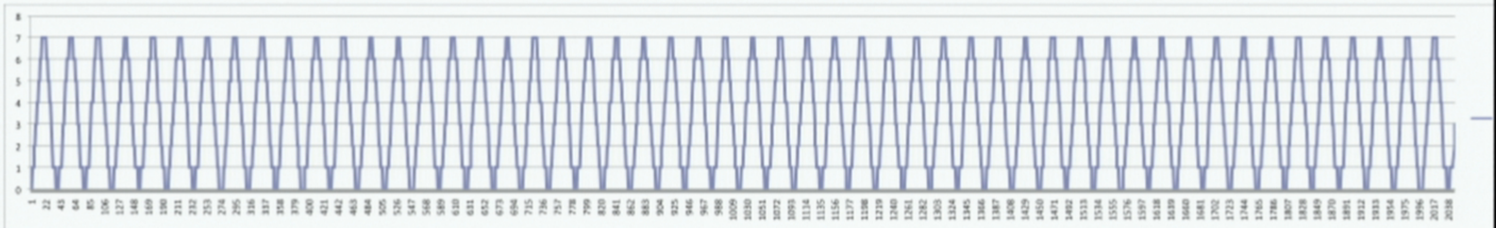
20 GS/s ADC based on Hittite HMCAD5831LP9BE

(with Rick Raffanti, same chip being used at CARMA by Dave Hawkins)

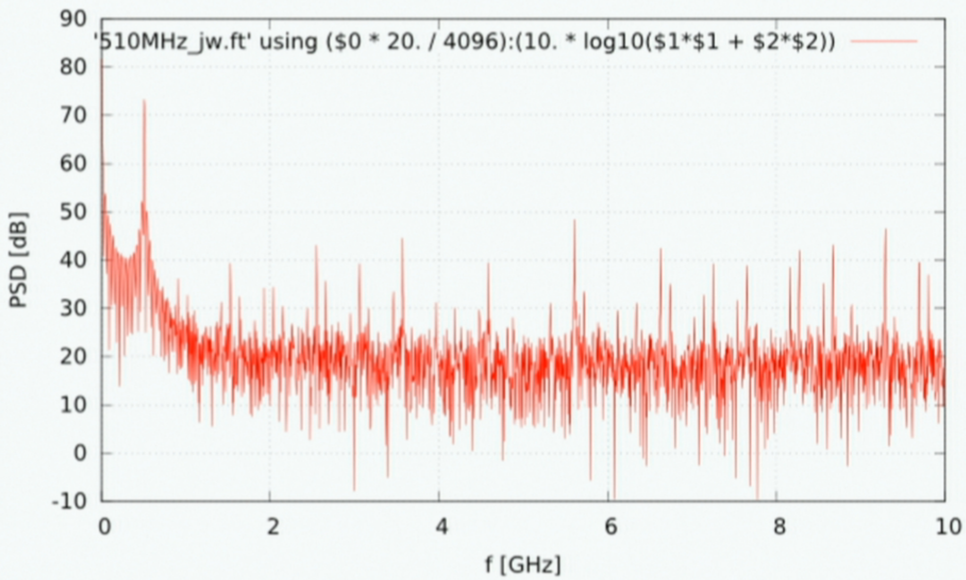


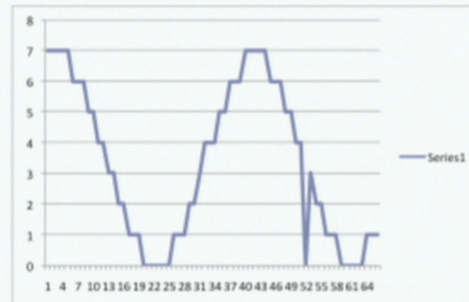
50 ps per sample! 510 MHz sine wave

snapshot of 510 MHz sine wave sampled at 20 GS/s to 3 bits resolution (50 ps sample interval!)



and FFT of snapshot, FFT shows SFDR ~ 24 dB

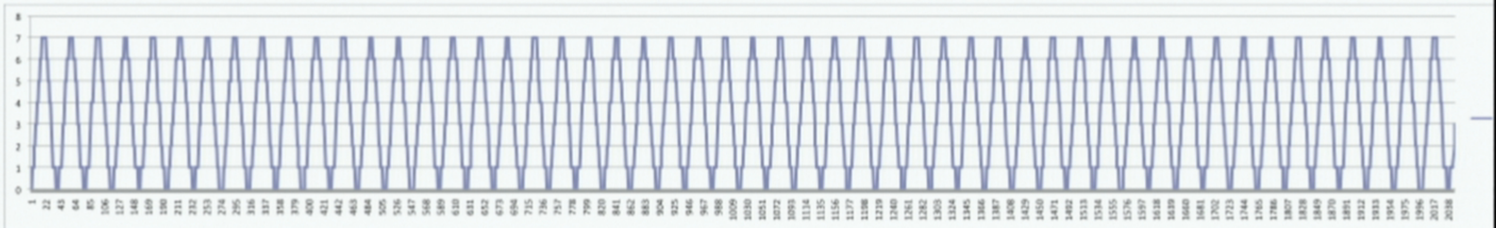




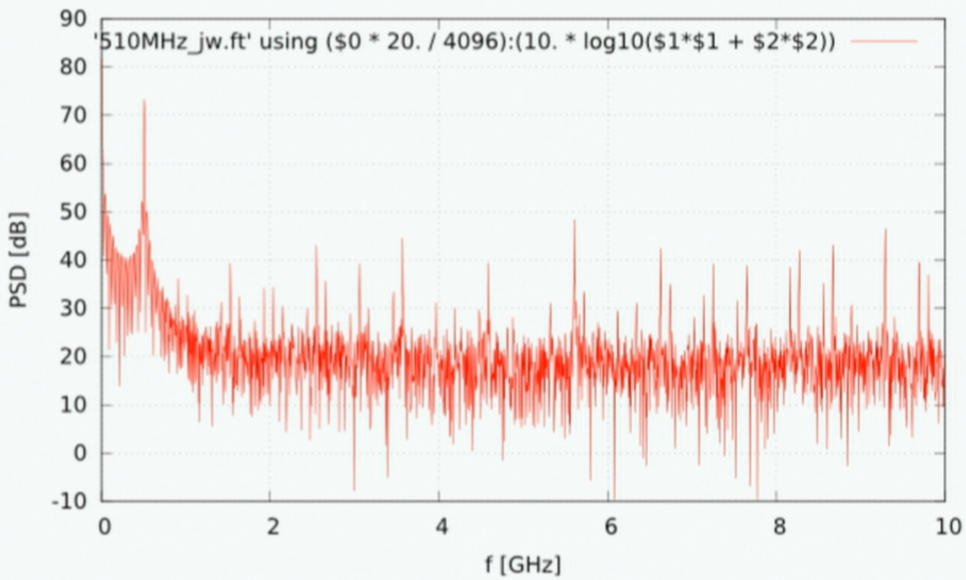
and a
1000
"norma
freque
note:

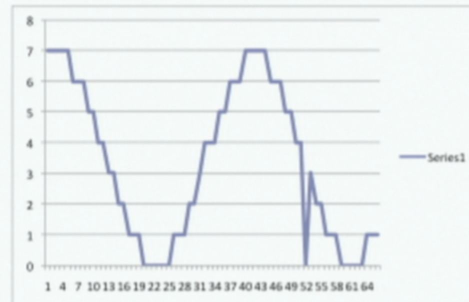
50 ps per sample! 510 MHz sine wave

snapshot of 510 MHz sine wave sampled at 20 GS/s to 3 bits resolution (50 ps sample interval!)



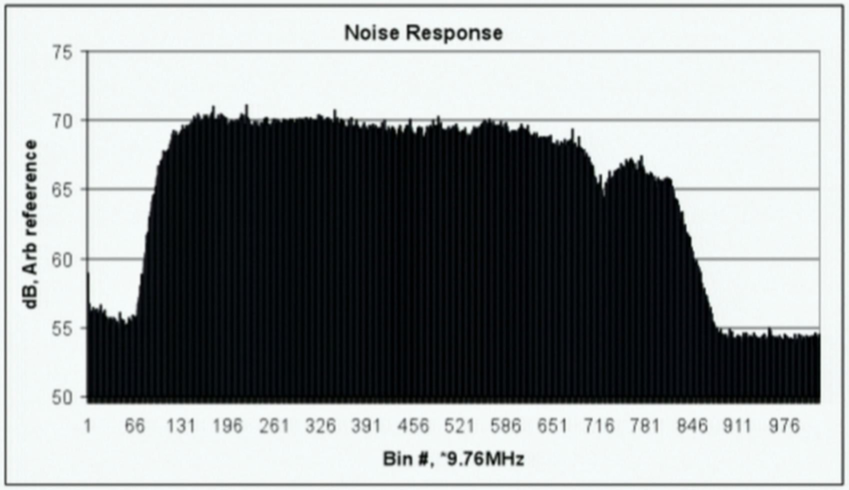
and FFT of snapshot, FFT shows SFDR ~ 24 dB



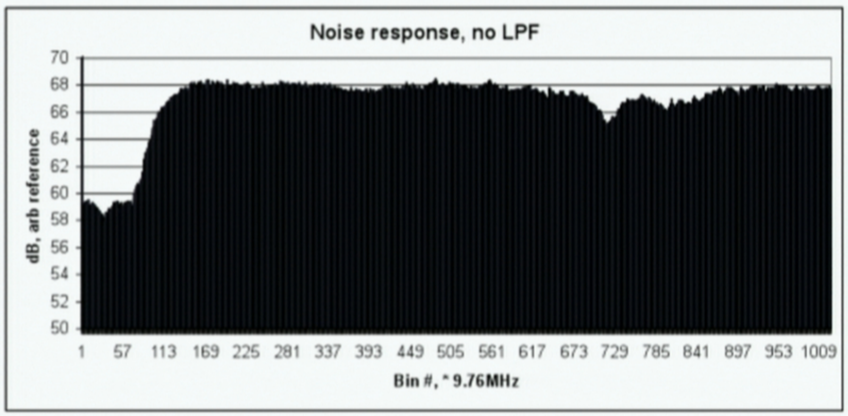


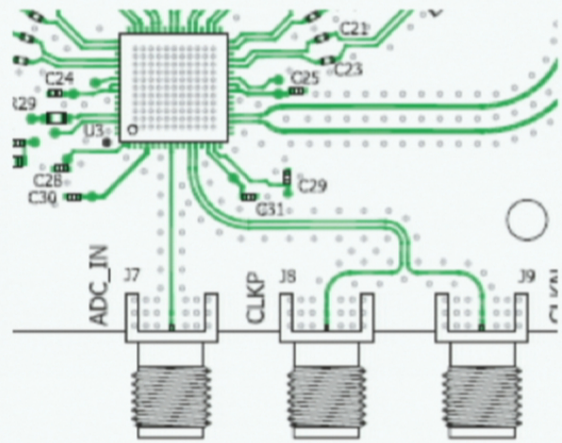
and a glitch every several 1000 points—“sparkle code” “normal” though more frequent than we’d like
note: not T/H on input

wideband noise, with and without 7.2 GHz LPF (18 GHz BW Noise Gen)

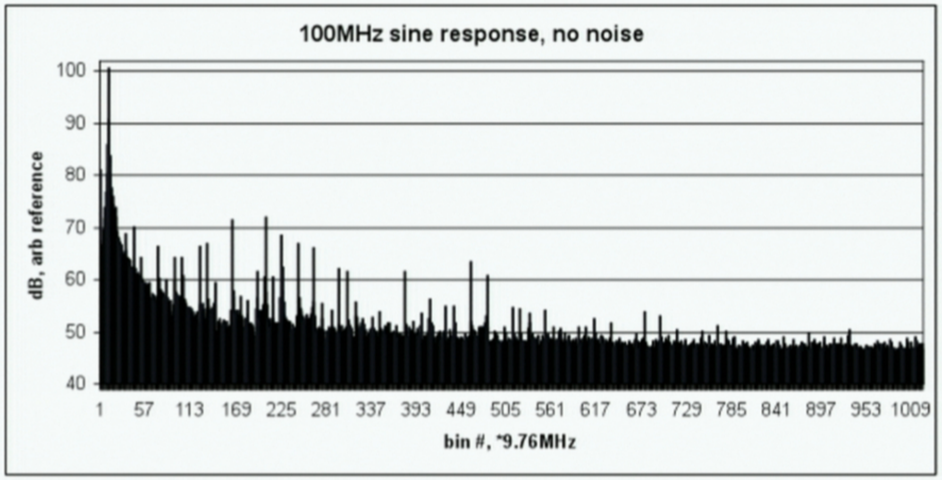


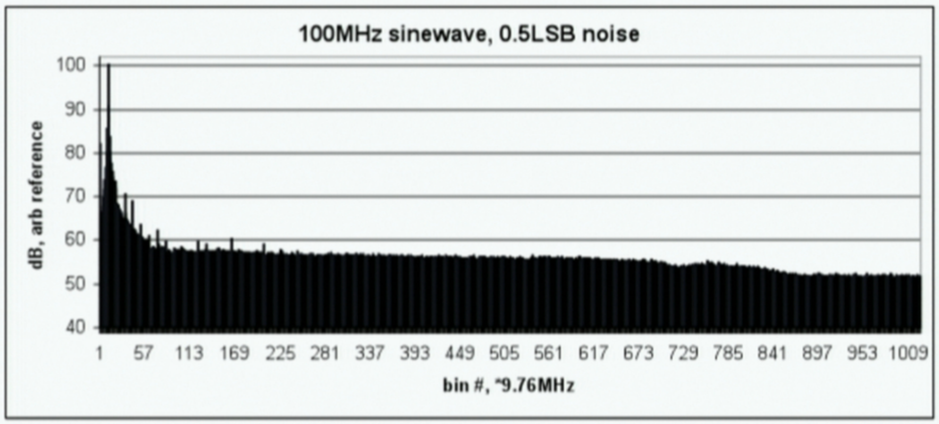
- 15 dB NPR as expected for 8 levels
- Passband decently flat to 10 GHz.
- Could dip at ~7 GHz be PCB response? Layout copied from eval board





dithering 100 MHz sine wave with noise improves SINAD





No noise:
ENOB ~ 3 bits
corresponds to
SINAD ~< 20 dB
SFDR = 28 dBc

Event Horizon Telescope Collaboration

(we need to standardize this page!)

DSP/EHT Instrument Team: R Primiani, L. Vertatschitsch, N. Patel, K. Young, R. Wilson, A. Young, J. Test, D. MacMahon, R. Raffanti, P. Yamaguchi, J. Weintroub,

CASPER Collaboration: https://casper.berkeley.edu/

SAO: S. Doeleman, M. Johnson, L. Blackburn, A. Chael, K. Rosenfeld, Nina ?

MIT Haystack: S. Doeleman, A. Rogers, V. Fish, R. Lu, J. SooHoo, M Titus, C. Beaudoin, R. Cappallo, G. Crew

NAOJ: Mareki Honma, Tomoaki Oyama, Kazunori Akiyama

U. Arizona Steward Obs & SPT: L. Ziurys, R. Freund, D. Marrone

CARMA: D. Plambeck, M. Wright, D. Woody, G. Bower,

NRAO: J. Webber, R. Escoffier, R. Lacasse, J. Greenberg

ASIAA/EAO/JCMT: G. Bower

UC Berkeley SSL / CASPER: D. Werthimer, D. MacMahon, M. Dexter

MPIfR: T. Krichbaum, A. Zensus, A. Roy

IRAM: M. Bremer, K. Schuster

APEX: K. Menten, M. Lindqvist

Radboud: H. Falcke, R. Tilanus

LMT, UMass: G. Narayanan, D. Hughes, …

ASIAA: P. Ho, M. Inoue, K. Asada

U. Concepcion: N. Nagar

questions?

EHT@SAO & SMA: R. Primiani, K. Young, D. MacMahon J. Test, B. Force L. Vertatschitsch, M. Johnson, L Blackburn, K. Rosenfeld, A. Young, R. Wilson, P. Yamaguchi, S. Doeleman, J Moran, D. Kubo, J. Weintroub