Title: VLBI Backend Systems

Date: Nov 13, 2014 02:30 PM

URL: http://pirsa.org/14110101

Abstract: The EHT data acquisition campaign in March 2015 will utilize new digital backends on many of the new and existing sites. We will briefly overview the state of the art for wideband digital backends for VLBI and discuss the several flavors that will be employed this coming year. Specifically, we will focus on details of the Roach2 Digital Backend (R2DBE), a new 16 Gbps wideband DBE unit that can be scaled to 64 Gbps, to be employed at single dish sites. The R2DBE digitizes 2.048 GHz of RF in each of two inputs and sends 8 Gbps single-channel data on each of two 10 GbE links to a Mark 6 data recorder with expansion chassis for a total of 16 Gbps. The system utilizes open source hardware, firmware, and software developed through the Collaboration for Astronomy Signal Processing and Electronics Research (CASPER). Engineers at SAO have been members and developers for the CASPER group for several years, thus the challenge of rapidly prototyping a VLBI backend system on a limited budget and short time scale could be met by drawing on years of previous development and expertise. In four months the system was developed and demonstrated in 32 Gbps form for the South Pole Telescope, achieving fringes in a hybrid correlation between an R2DBE and an existing R1DBE. We present the tests and results achieved with the R2DBE 32 Gbps system for the South Pole, and upcoming developments in preparation for March 2015.

VLBI Digital Backends

Laura Vertatschitsch


PERIMETER
INSTITUTE
FOR THEORETICAL PHYSICS

Outline

Focus on ROACH2 Digital Backend (R2DBE) system

- Motivation for R2DBE
- Some details of R2DBE hardware, bitcode
- SPT 32 Gbps Digital Backend System
- SPT testing
- Future Development

Important, but not covered in this talk are details of the Block Downconverter IF system and the Mark6 data recorders

Motivation

- Goal: To outfit the single dish telescopes with a common digital backend system for EHT VLBI
- Increase sensitivity at 1.3 mm → Increasing BW
- Future
  - 4 GHz, dual pol, double sideband
  - 4 GHz *2 sidebands * 2 Nyquist * 2 bits * 2 polarizations
  - 64 Gbps
- March 2015
  - 2 GHz, dual pol, single sideband
  - 16 Gbps
- R1DBE too old, DBBC3 too new
- Need a system that fits – technology exists, let's build it
  - R2DBE will do 16 Gbps, can be scaled to 64 Gbps

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Major Drivers

Challenges	Advantages
▪ SPT Timeline → Simplicity ▪ SPT: 32 Gbps ▪ Cross-correlation validation ▪ Time on the Sky	▪ Access to sites for VLBI testing ▪ DBE design experience at Haystack/SAO ▪ Equipment experience ▪ Open source development tools and experienced designers

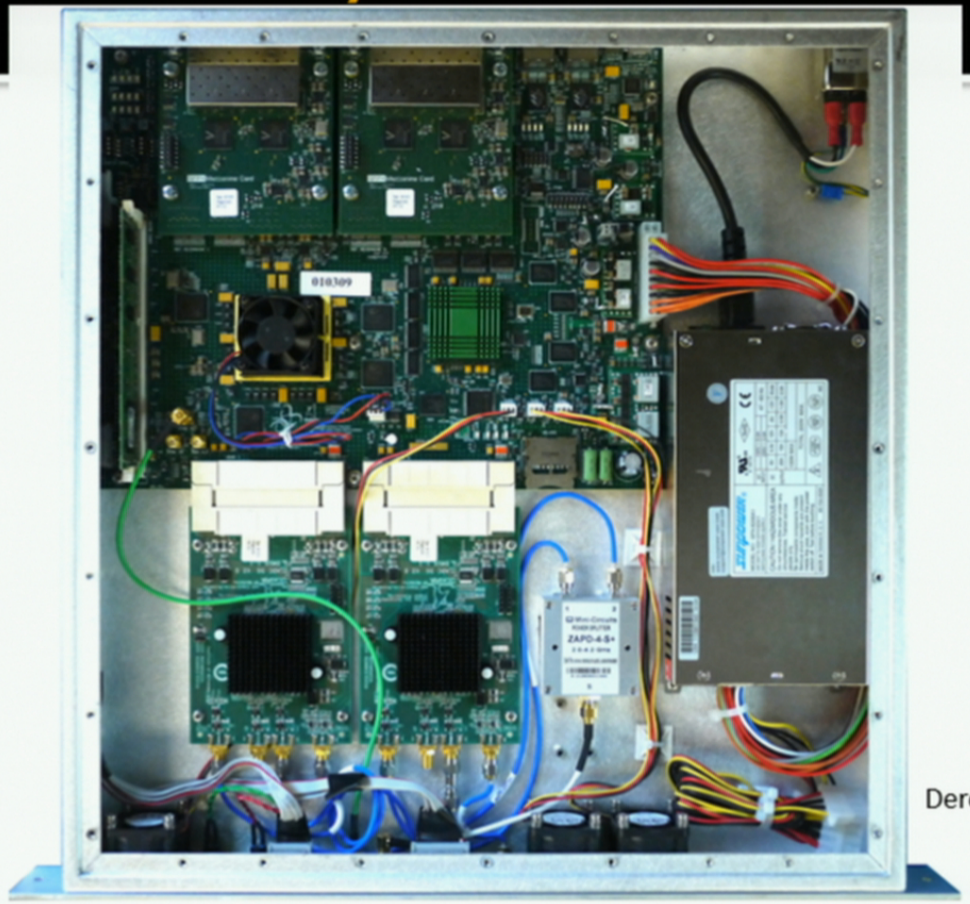
CASPER

Collaboration for Astronomy Signal Processing and Electronics Research

- Hardware
  - Reconfigurable Open Architecture Computing Hardware (ROACH)
  - Roach1, Roach2, Xilinx Field Programmable Gate Arrays (FPGAs), various ADC boards, Mezzanine Cards
  - SWARM, SKA, PAPER, VEGAS, Manastash Ridge Radar
- Software (Python)
- Firmware (HDL, Xilinx)
- High-Level Development Environment
  - Simulink+Matlab, high level block design with HDL under the hood

R2DBE Assembly

Top View

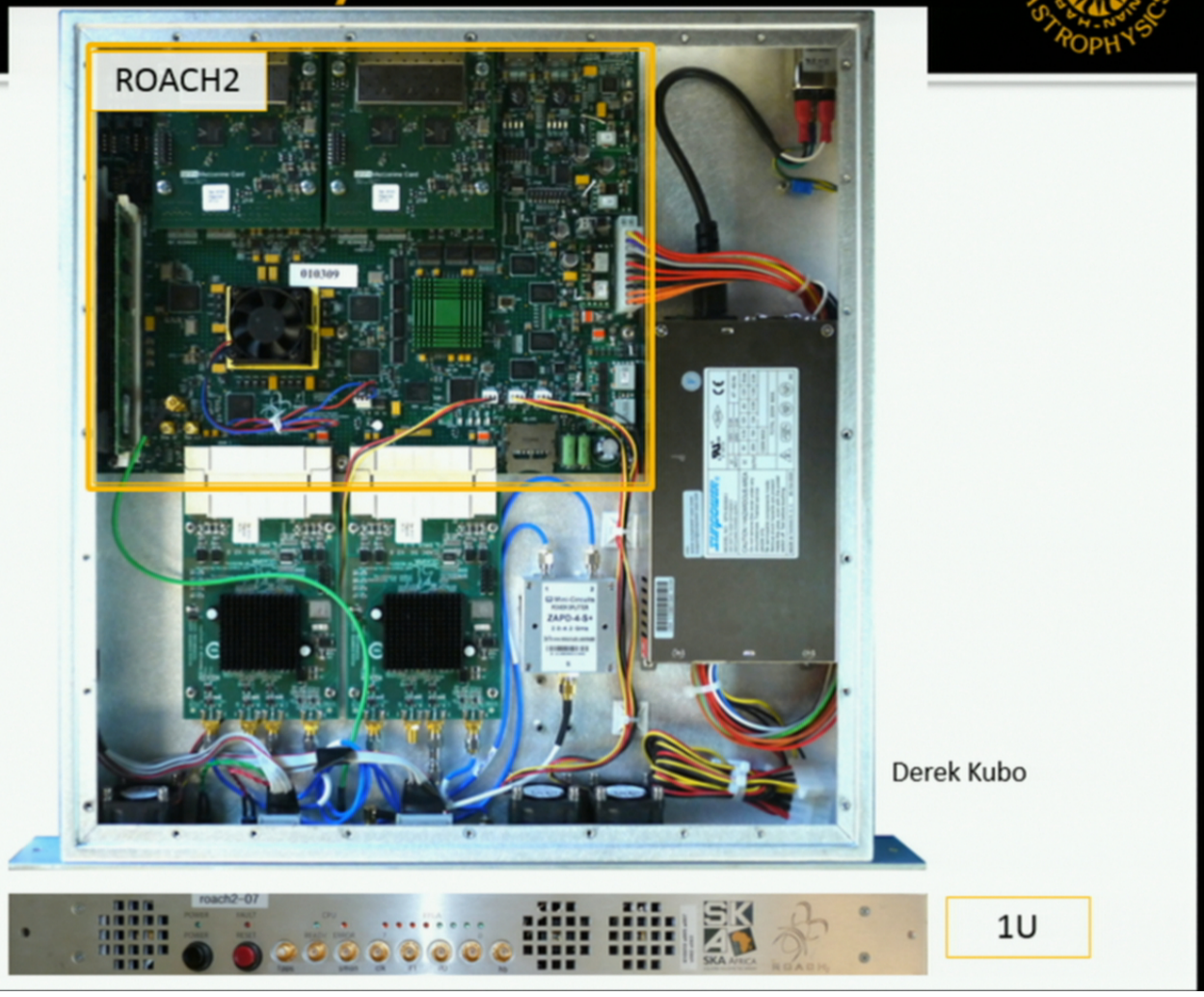


Derek Kubo

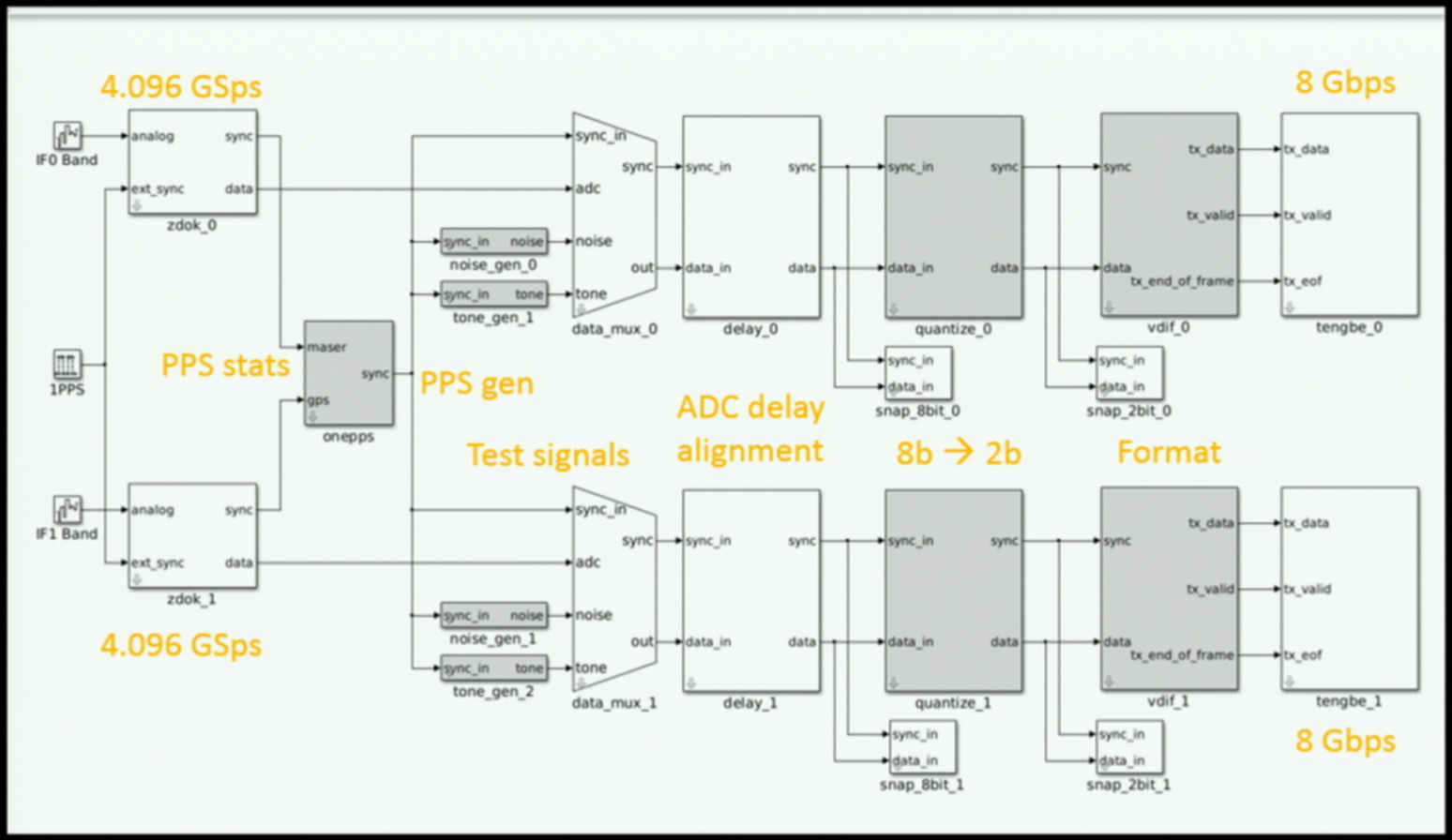
Front

1U

R2DBE Assembly



R2DBE – basic bitcode

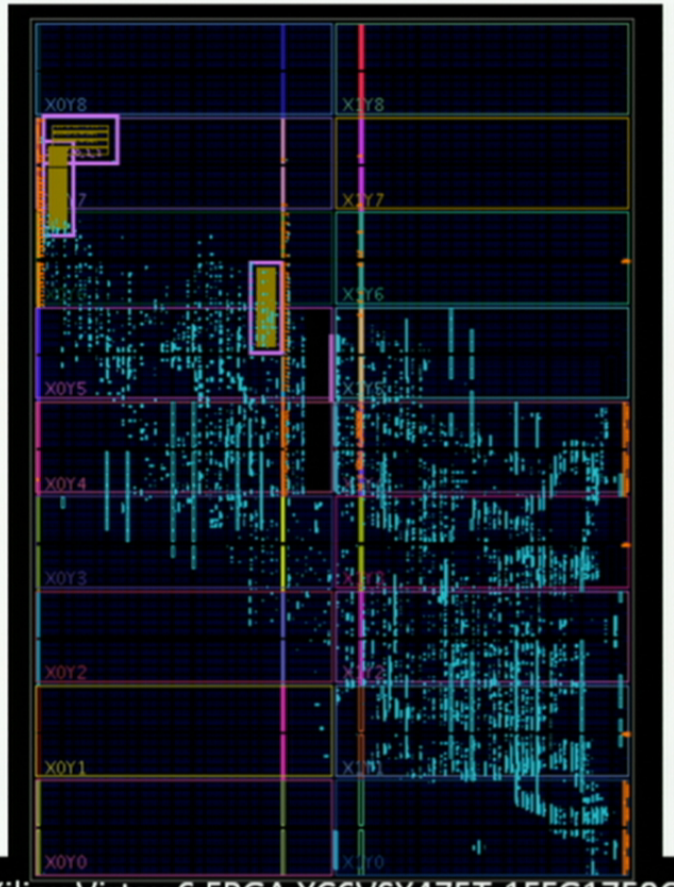


R2DBE – Bitcode Resource Usage

```
Compile Time:     1.75 hours
FPGA speed:        256 MHz
ADC sample rate: 4096 MSps
Data Rate out:     16 Gbps (2x10GbE)
```

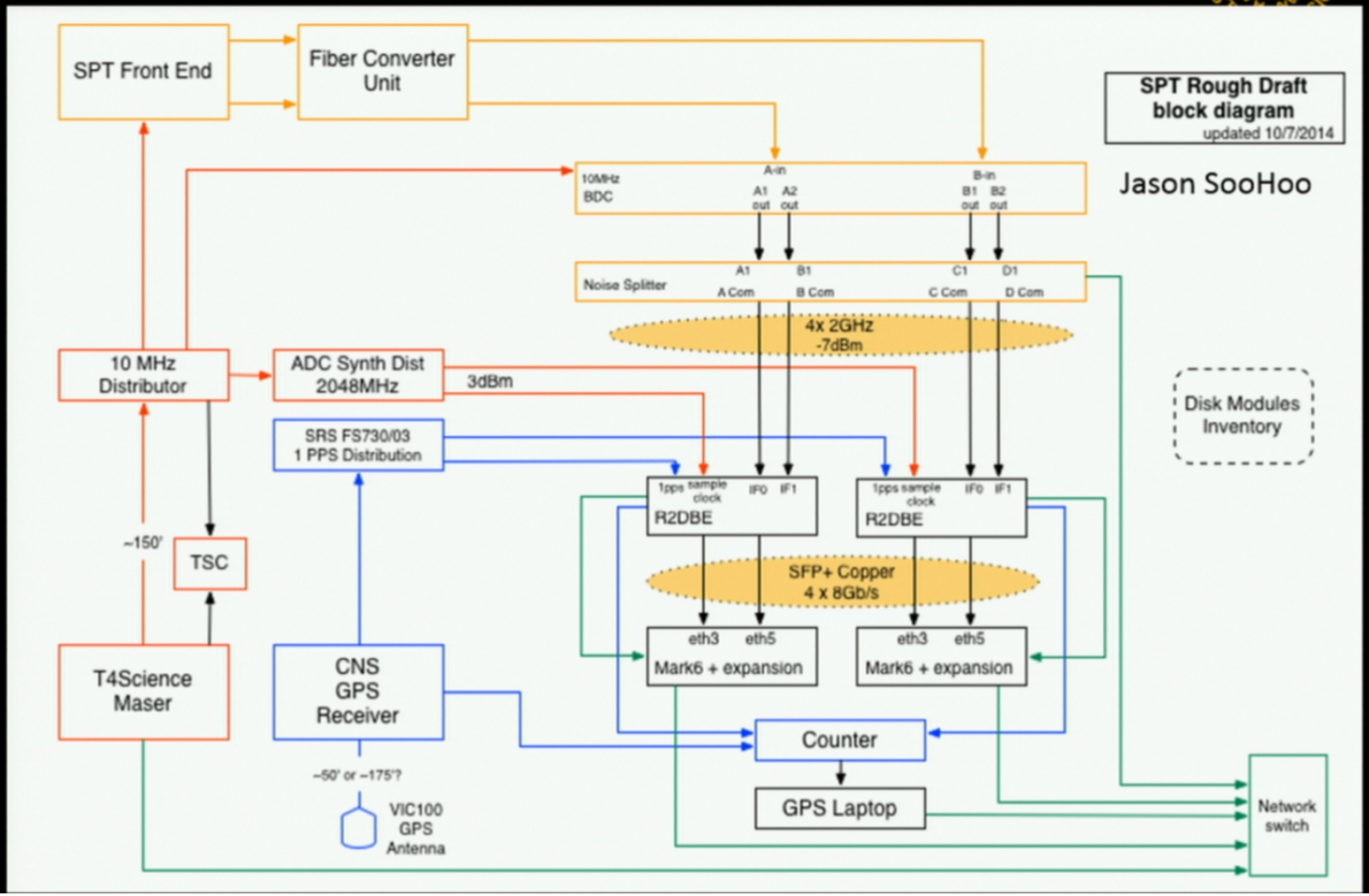
Resource	Usage
Occupied Slices	12%: 9,349 of 74,400
DSP48E1s	1%: 34 of 2,016
RAMB36E1	17%: 182 of 1,064
RAMB18E1	3%: 66 of 2,128
IO Utilization	27%: 232 of 840

Rule of thumb: 50% Resource Utilization



Xilinx Virtex 6 FPGA XC6VSX475T-1FFG1759C

Example: 32 Gbps SPT system



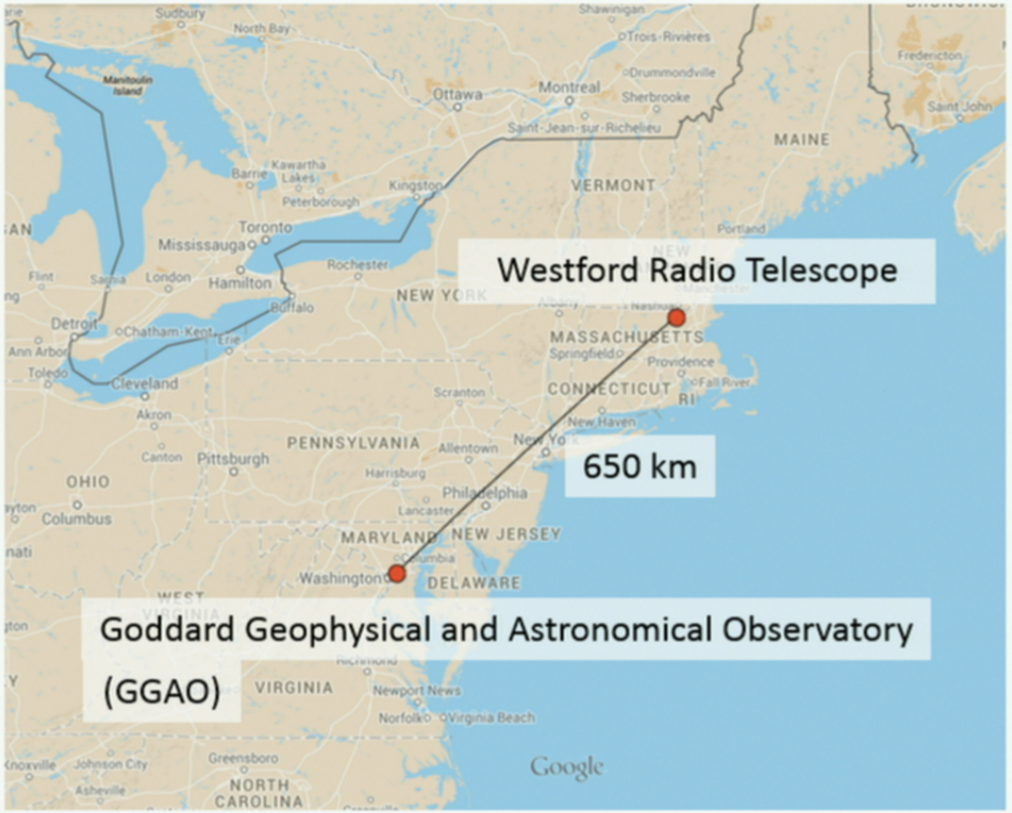
SPT testing strategy

- Test each module on the bench
- Build up SPT system at Wf
- Test Zero baseline R2-R2, R1-R2
- Test VLBI baseline Wf-GGAO
- Pack and Ship system from Wf
- Continue bitcode improvement

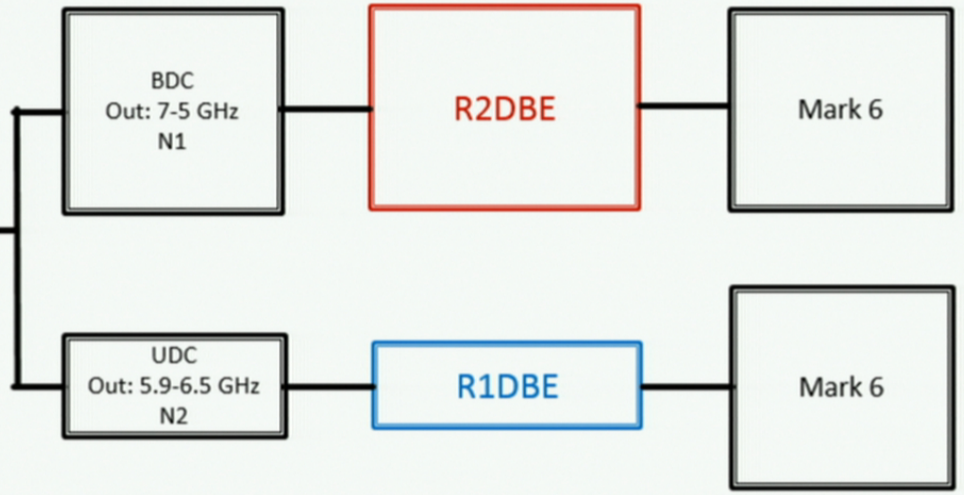
Westford SPT installation on Sept 12th, 2014
Laura Vertatschitsch, Arthur Niell, Jonathan Weintroub, Geoff Crew, Rurik Primiani

Sky Test Plan

- Wf-GGAO = 650 km
- Wf: R1,R2
- GGAO: R1
- Zero Baseline
  - R1 - R2
- VLBI test
  - R1 - R1
  - R1 - R2
- SX Wideband Receivers (~5 cm)
- 650 km (13 Mλ)
- Target: 4c39.25



Sky Test Freq Domain Map



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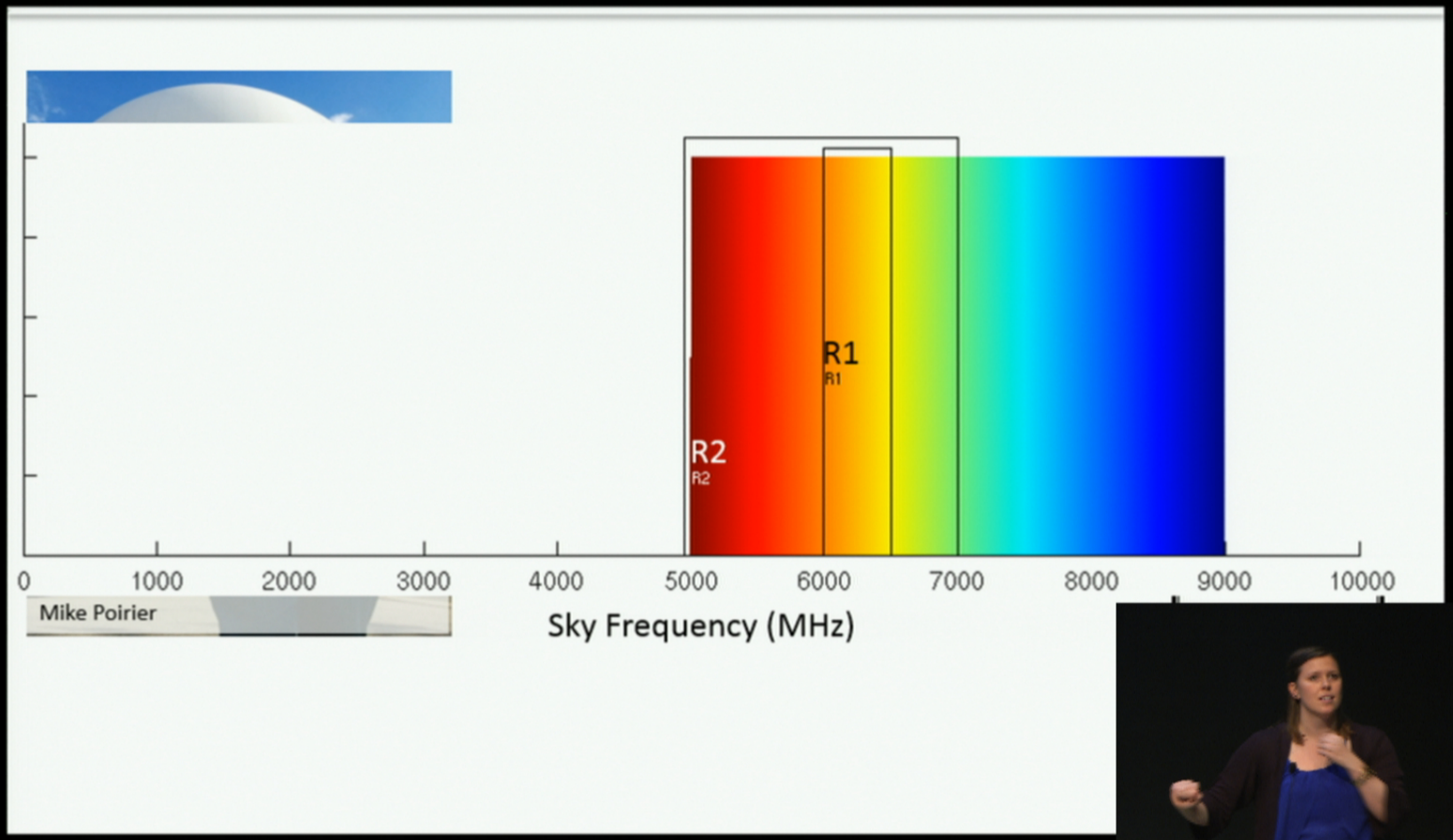

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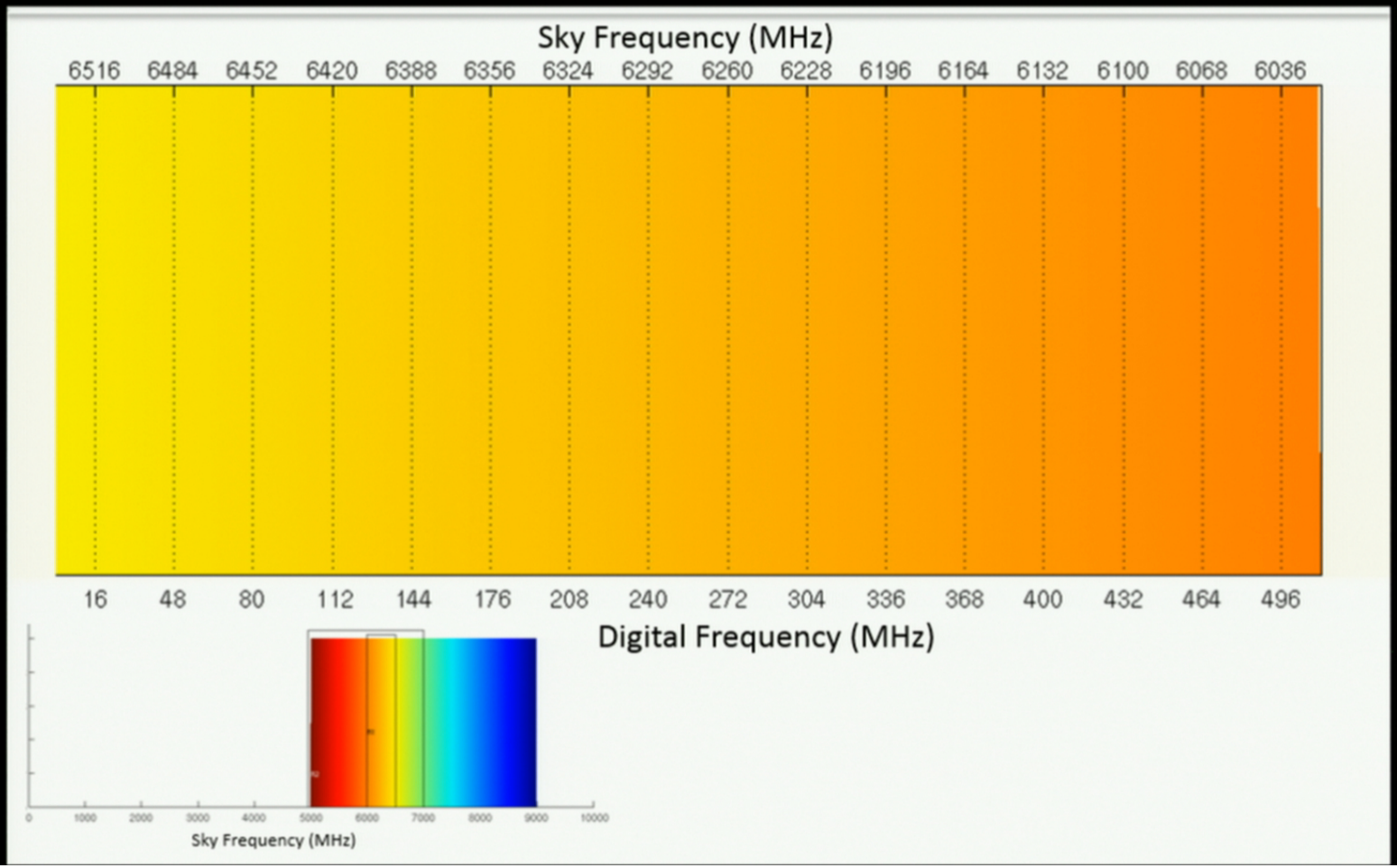
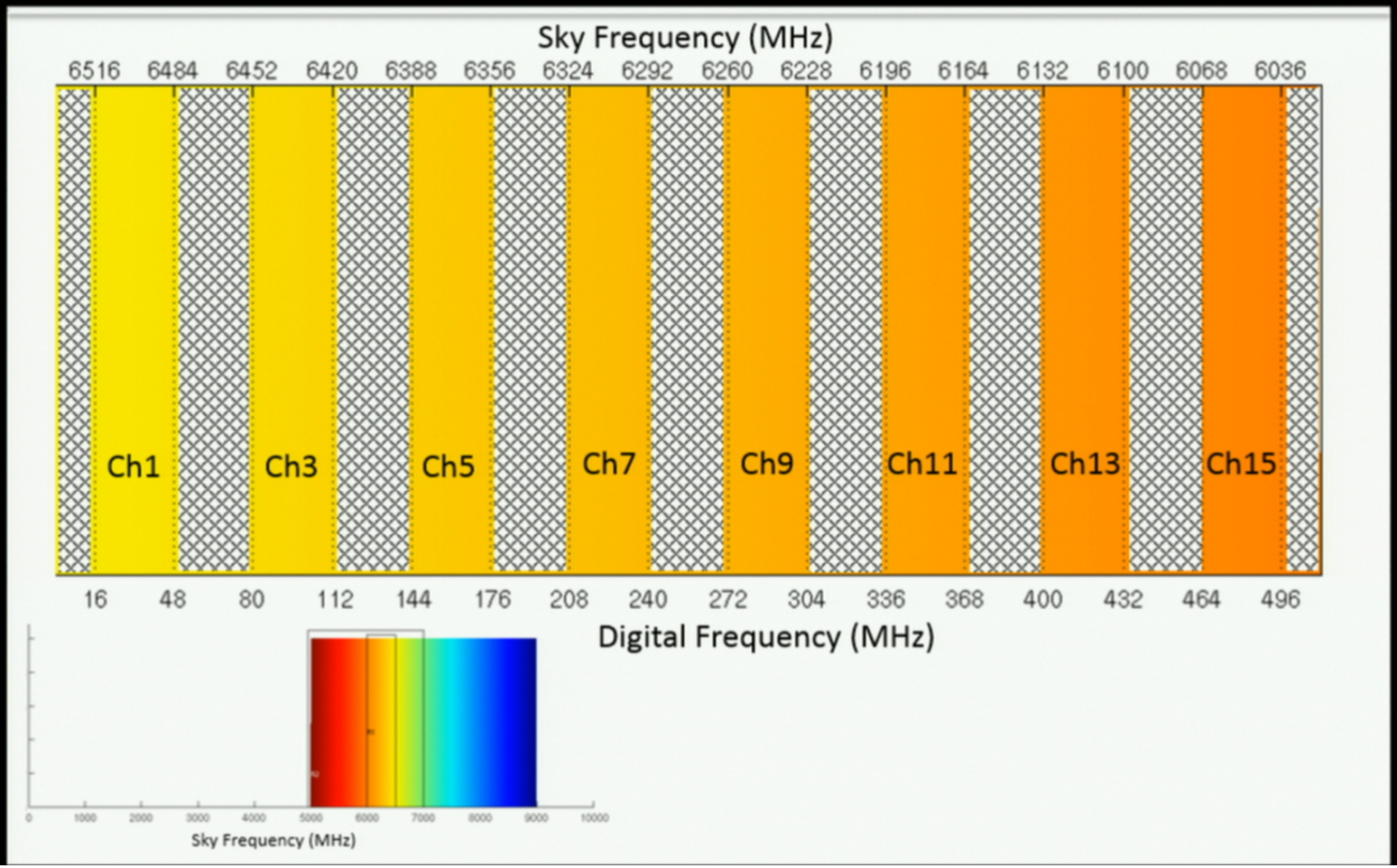
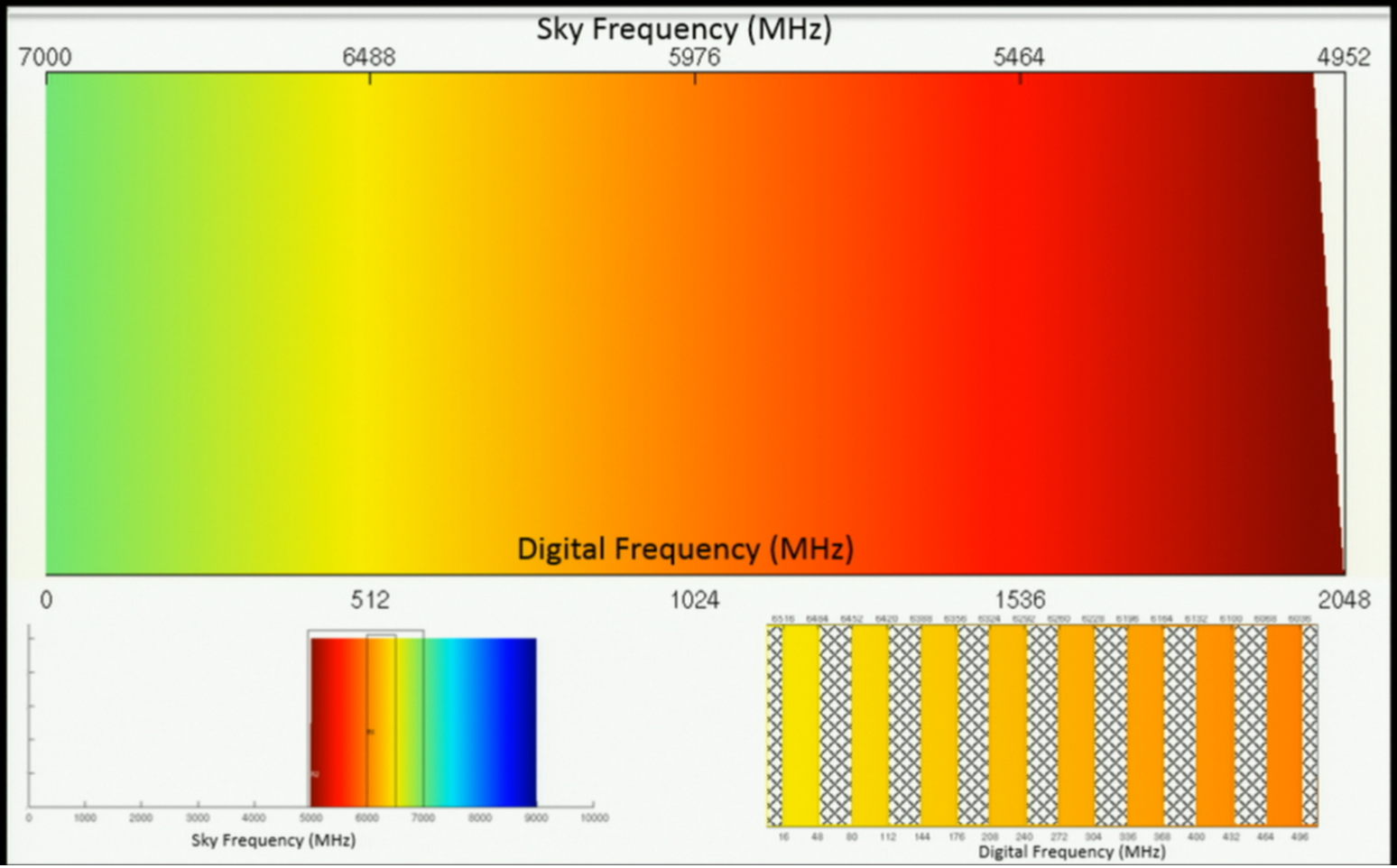


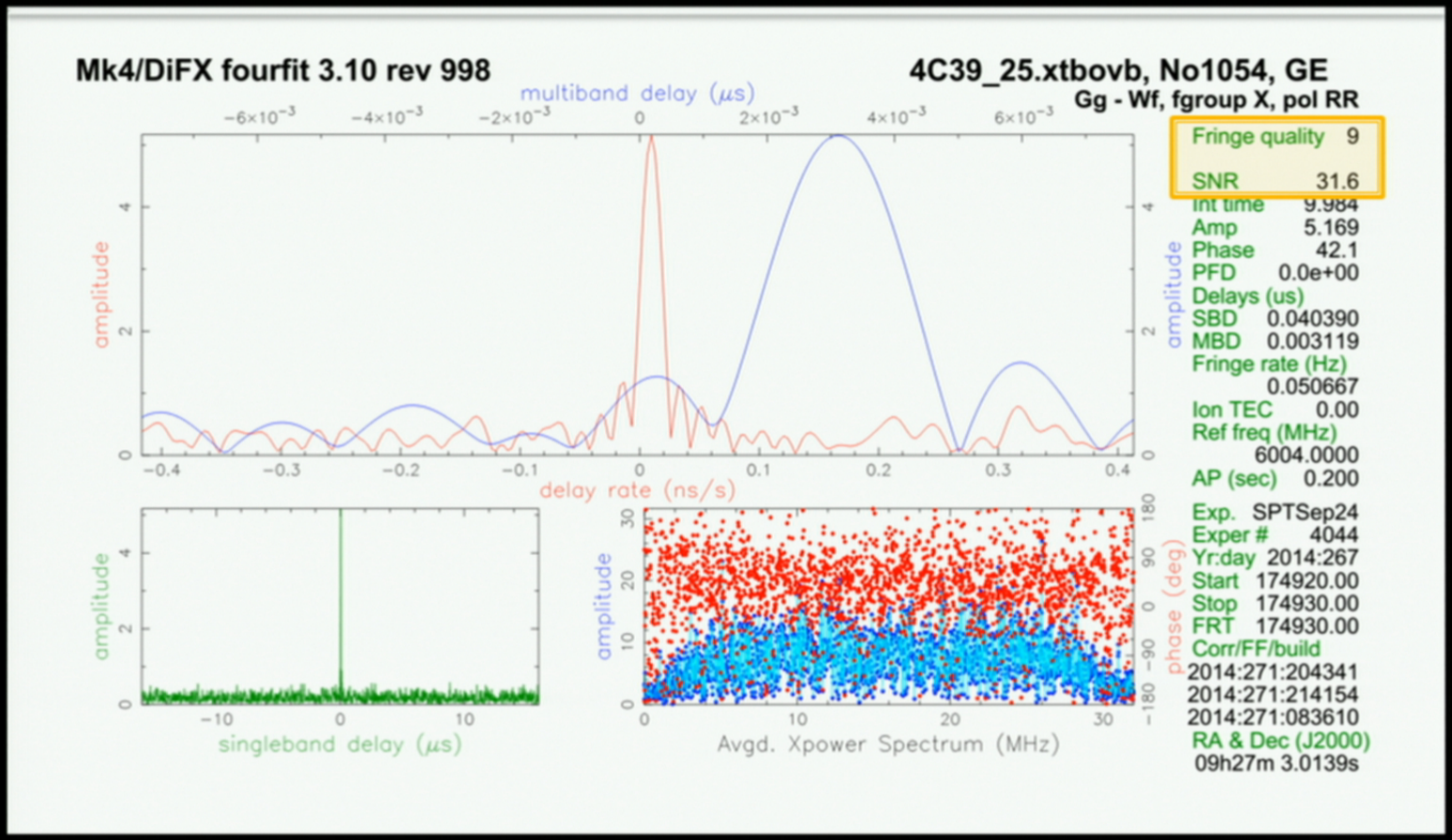
Sky Test Freq Domain Map



Sky Test Freq Domain Map



Sky Test Results: R1-R1 cross SNR 31.6



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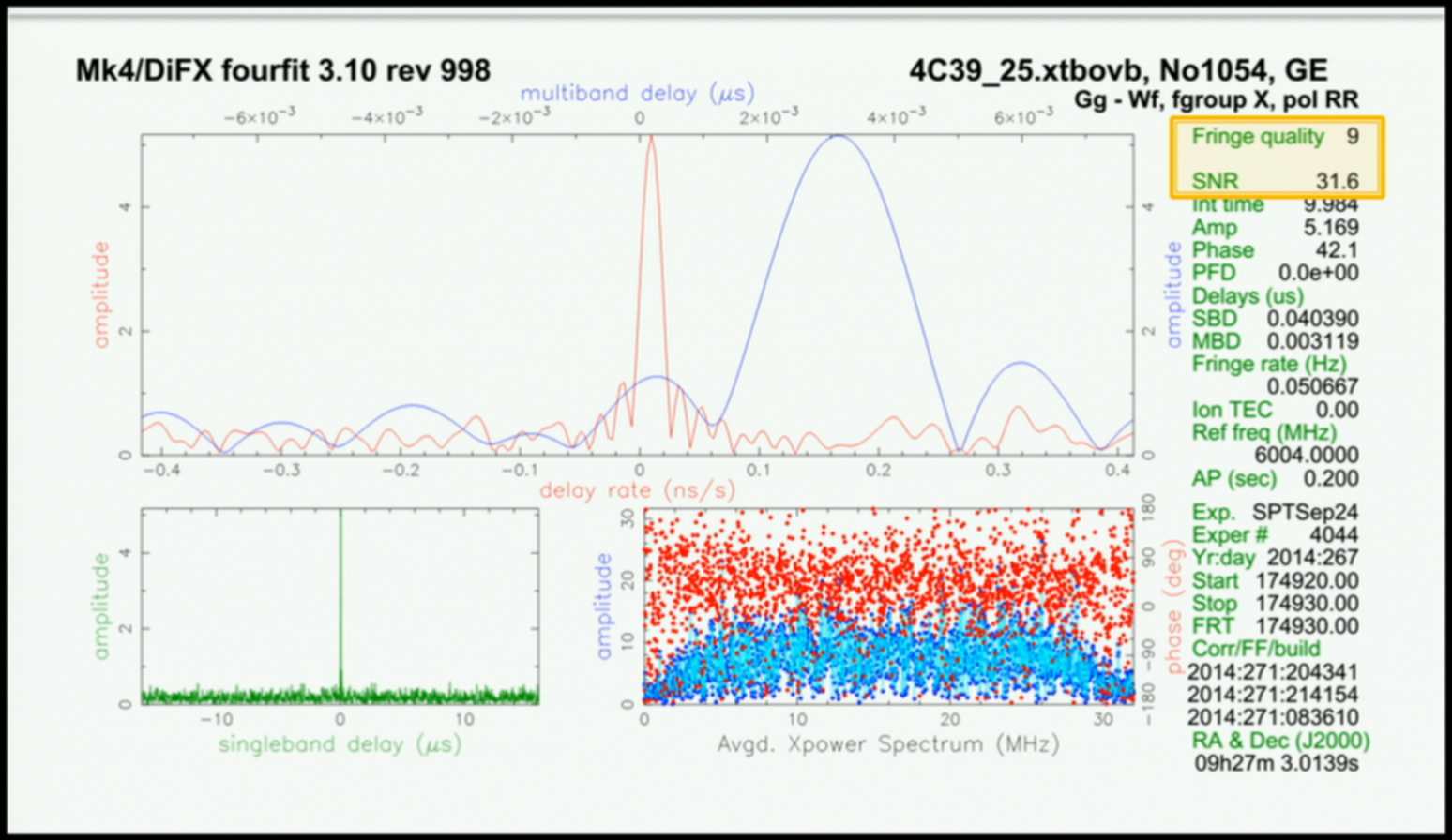
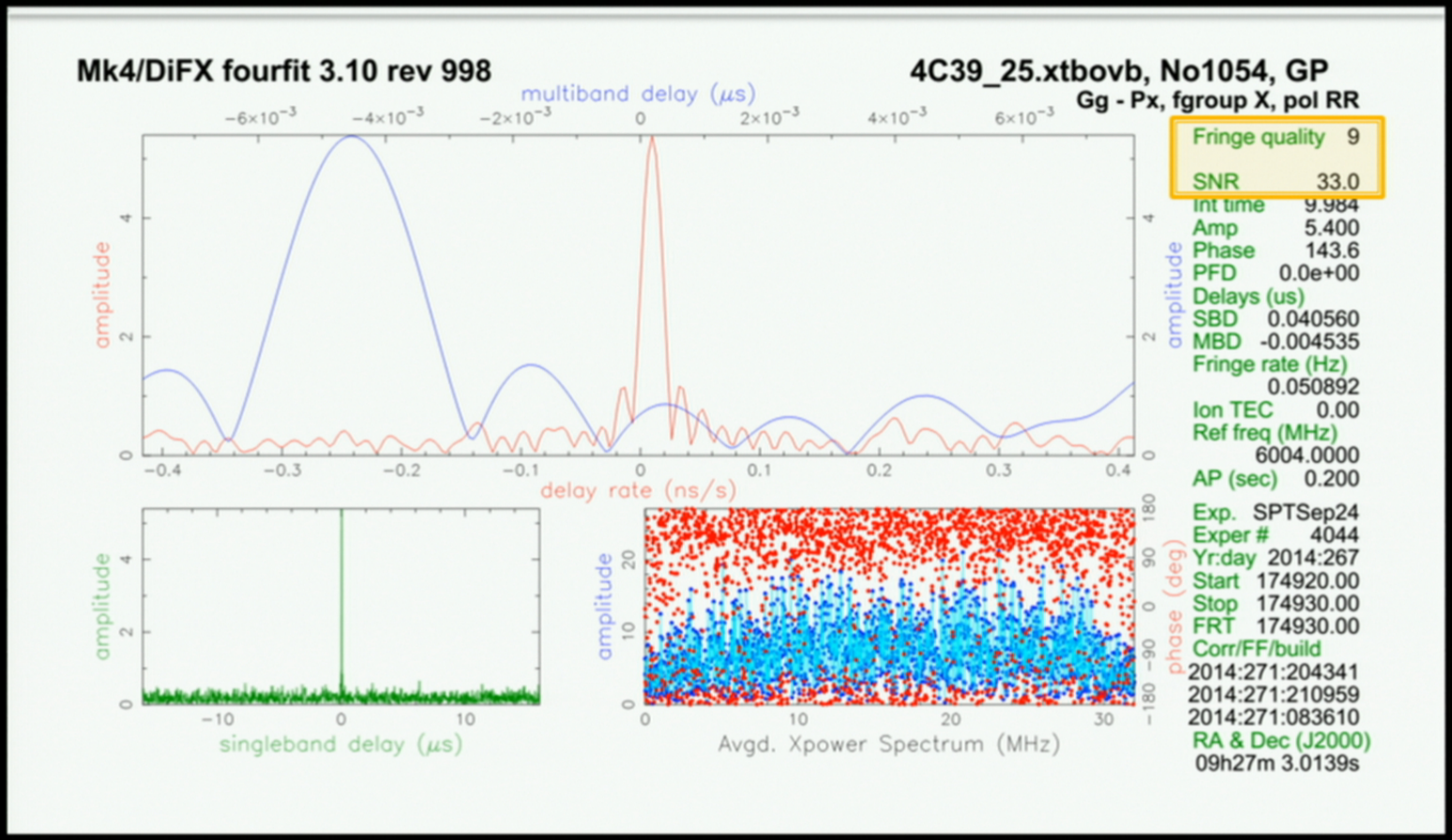
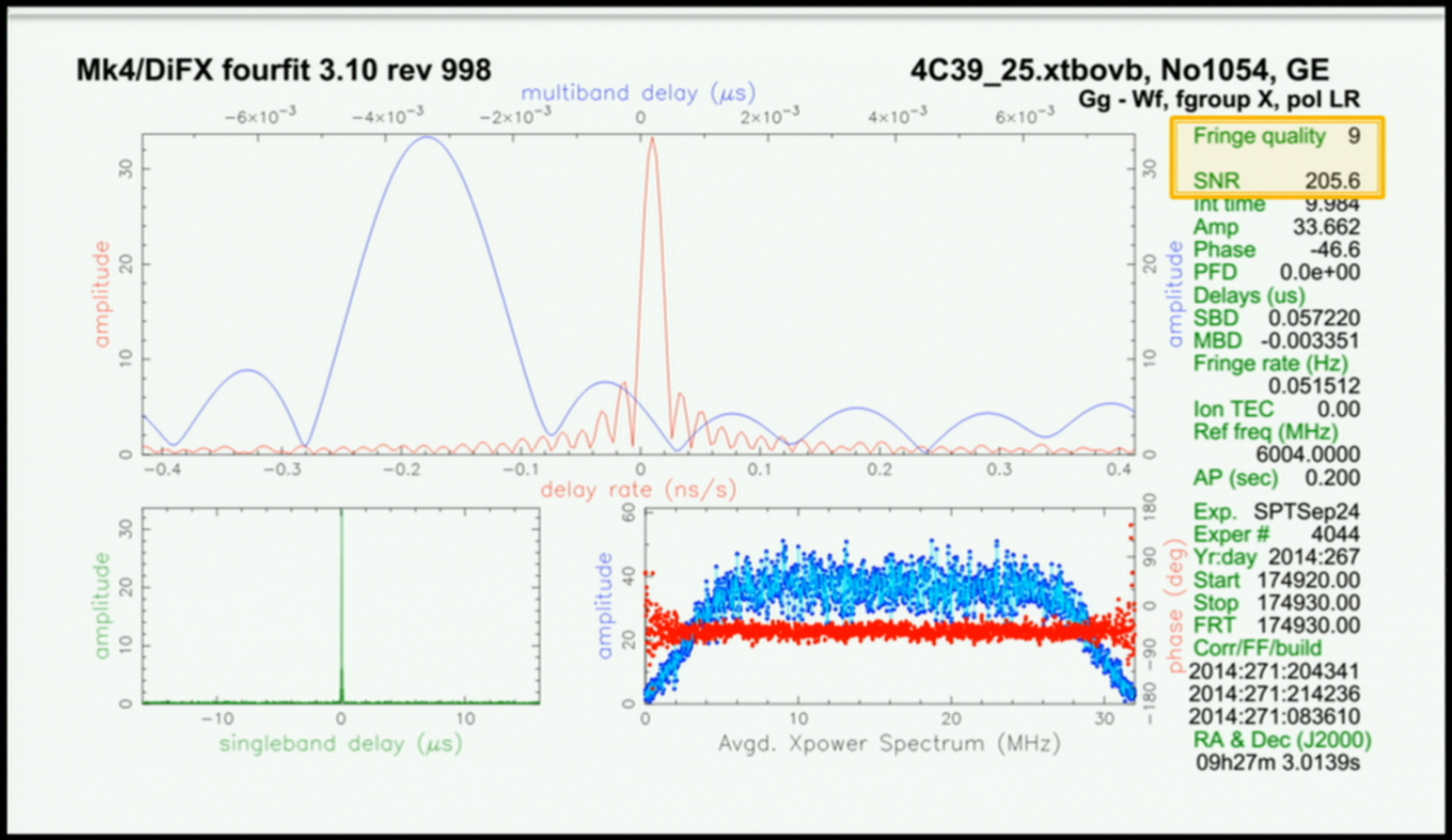


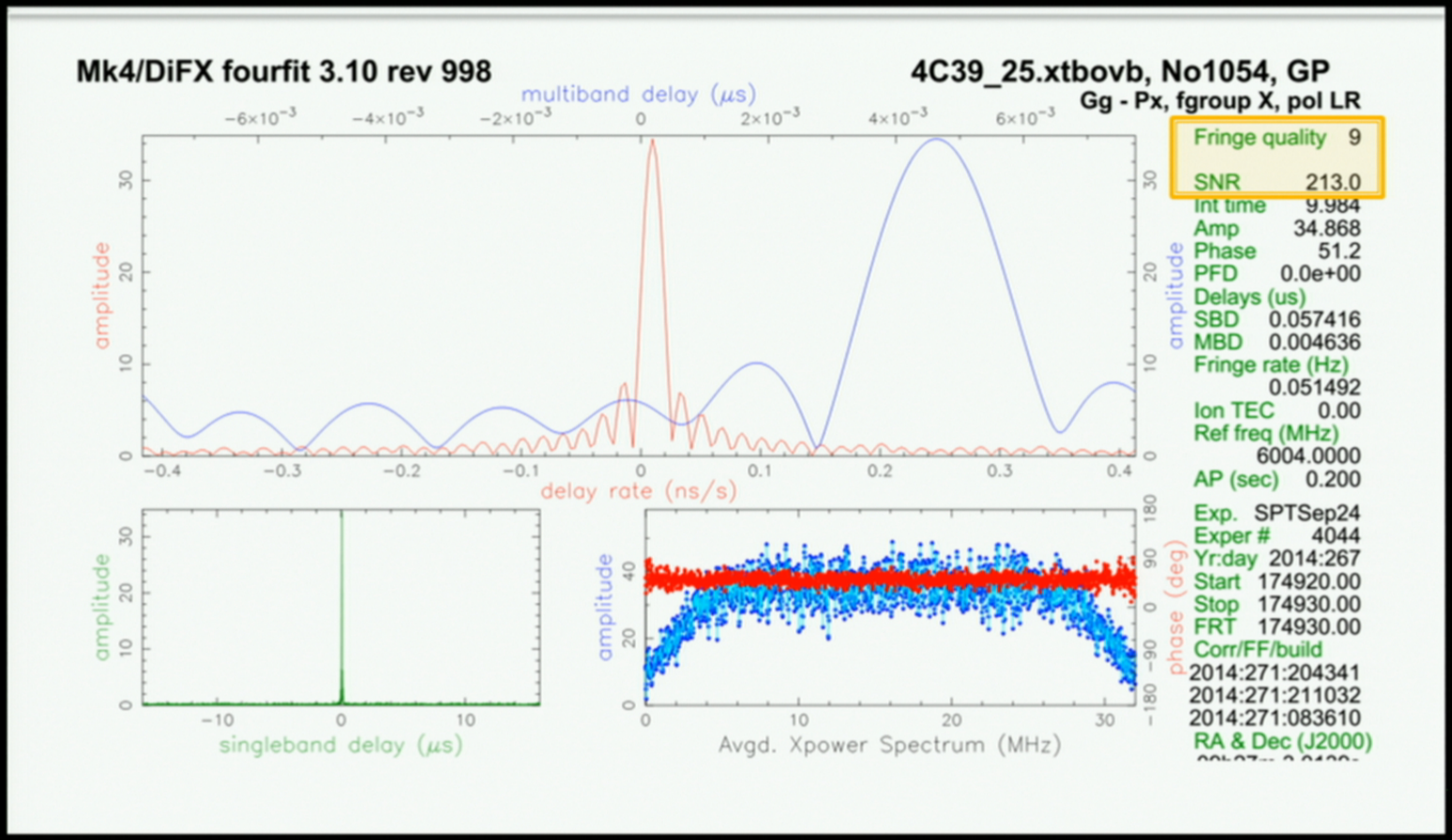
Sky Test Results: R1-R2 cross SNR 33.0



Sky Test Results: R1-R1 parallel SNR 205.6



Sky Test Results: R1-R2 parallel SNR 213.0



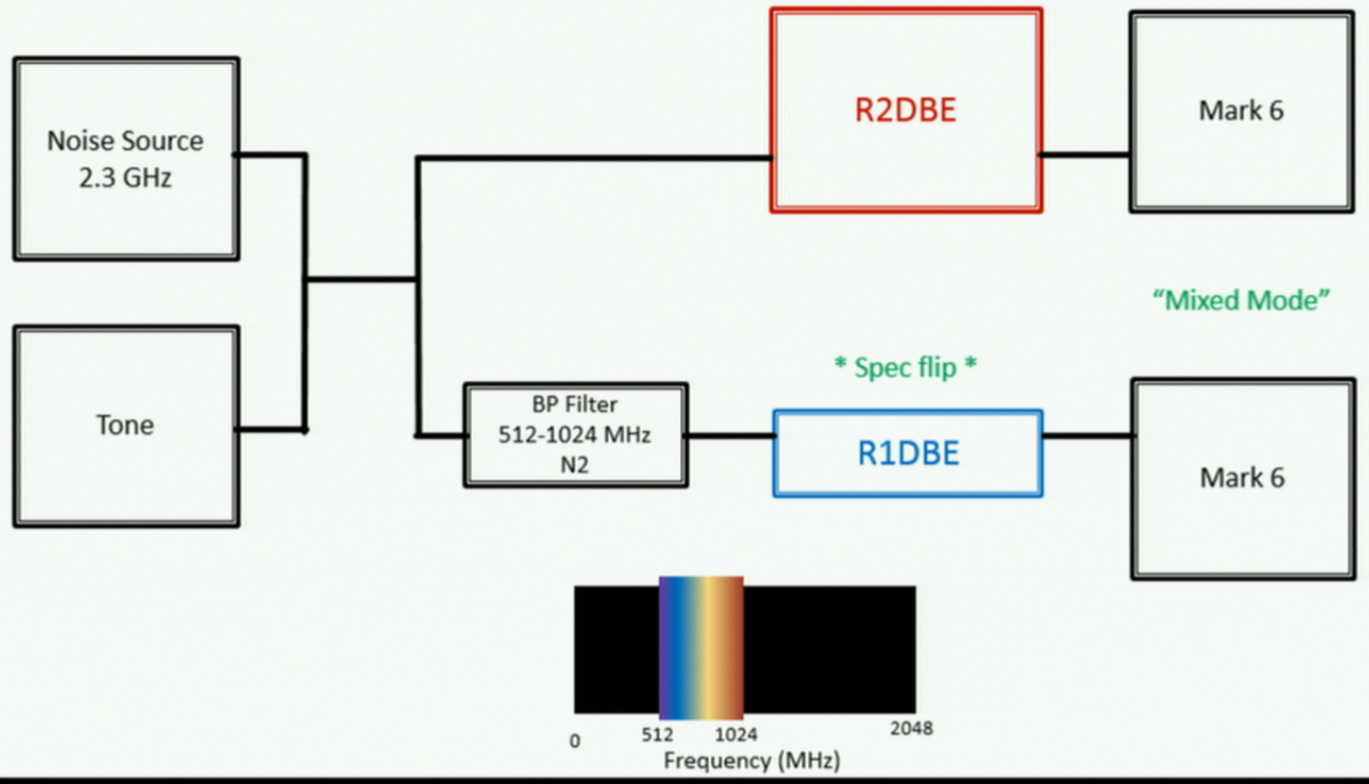
Start to Finish

Initial technology search: Feb 2014

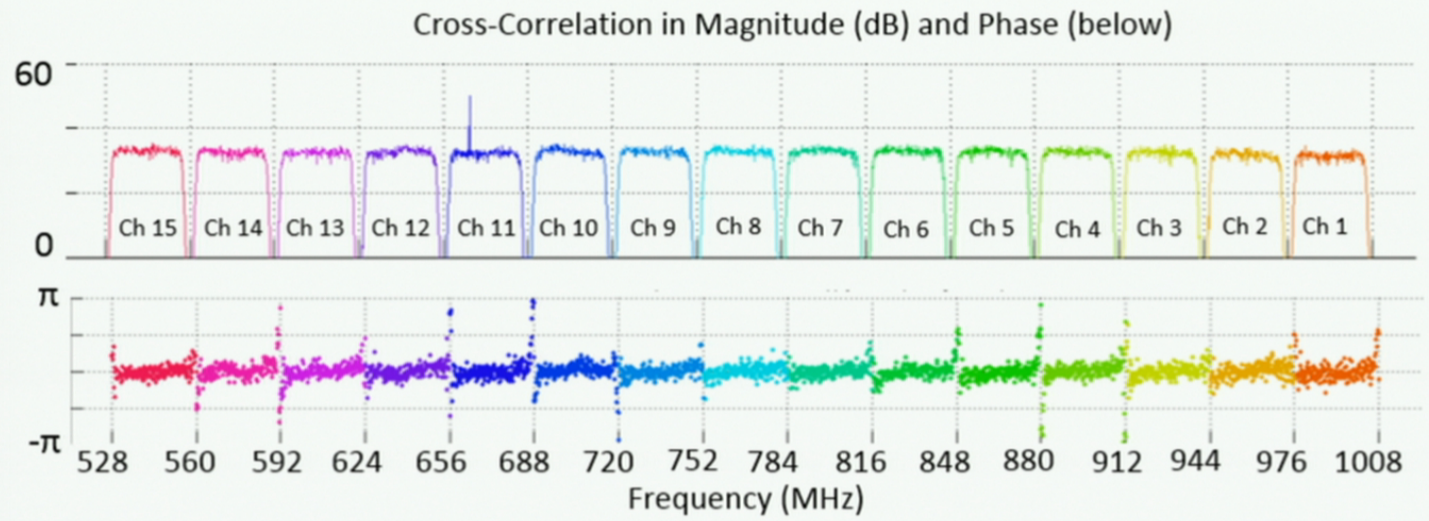
Start of development: July 2014
Ship to SPT: October 2014

Zero Baseline for Delay Estimation

Time offsets in R2DBE bitcode, corrected and SAO lab tested



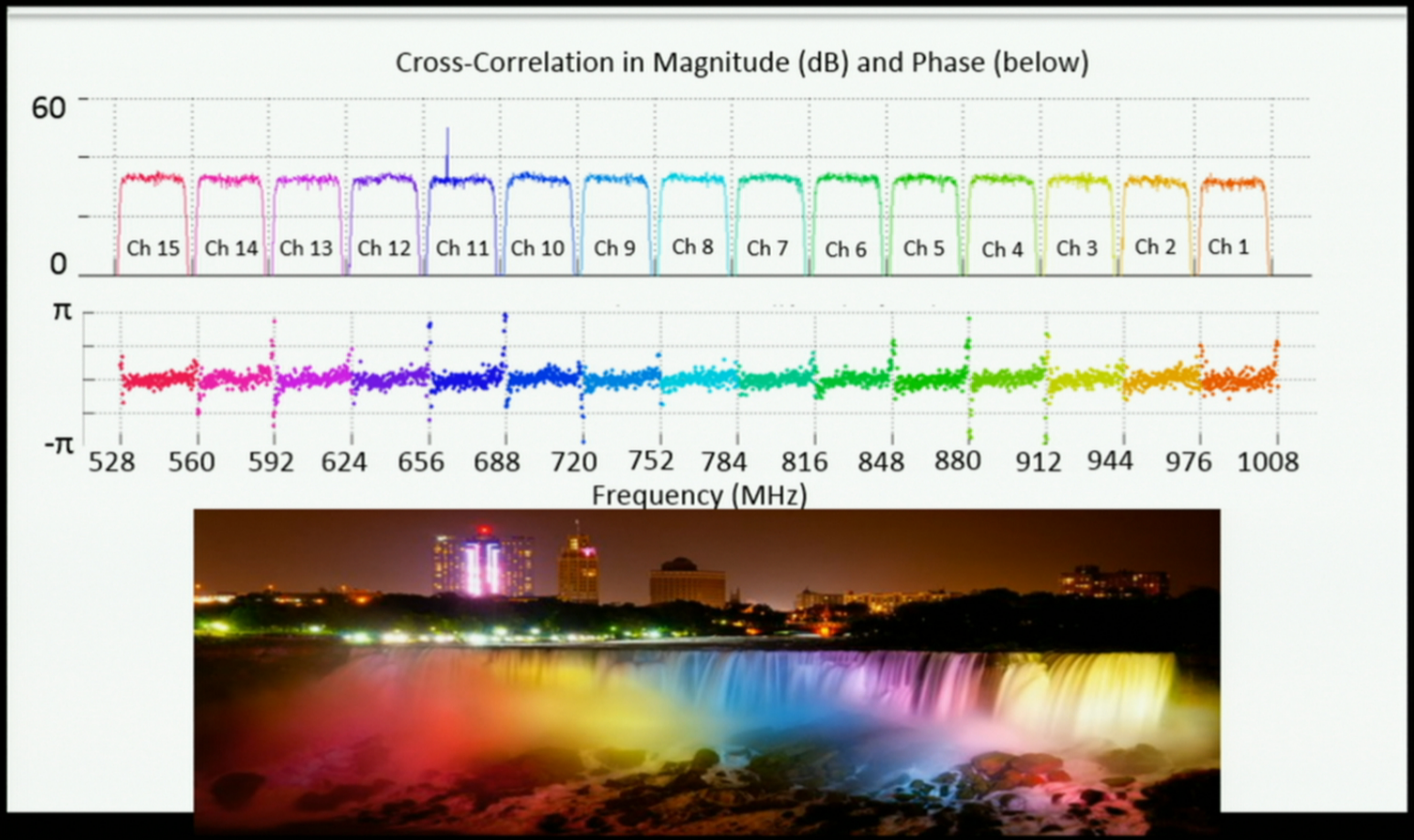
Zero Baseline Results



After correcting for drift in external PPS signal, R1DBE and R2DBE consistently correlate with delays ~100 ns (6-7 samples in the R1DBE)

In other words: R2DBE time is now trustworthy

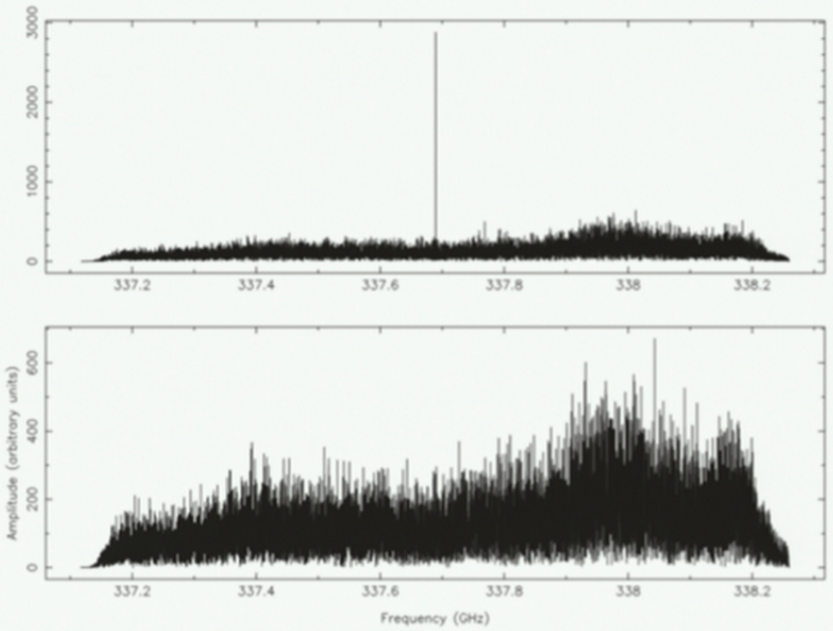
Zero Baseline Results



Sam S. "Niagara Falls in rainbow colors at night." www.yelp.com

Continued Improvement

- ADC calibration
- Software, Documentation
- Quantization
  - Pre-whitening before ADC (correct for 6 dB slope)
  - Implement optimal 2-bit quantization, DC offset
- Embed Statistics in VDIF Headers
  - Thresholds, GPS/Maser offset
- 2.0 GHz sampling mode (matching ALMA)
  - FPGA runs at 250 MHz
  - Digital PPS creation adjusted for new rate
- PFB implementation
  - Resource usage is small



Patel, et al, 2014

Summary

Goal: Build digital backend for EHT single dish stations, with intent to deploy for March 2015, scalable to full 64 Gbps

What we did

- Designed, tested and shipped to the SPT
  - Designed
    - SPT shipping deadlines required rapid prototyping and development → simple bitcode (INITIALLY)
  - Tested
    - Demonstrated fringes on the sky with the SPT system (R2DBE vs R1DBE)
    - Demonstrates zoom-band correlation capabilities necessary for March 2015 single dish vs phased array correlation
  - Shipped
    - Gives us shopping list for other sites

What we will do

- Continue to improve bitcode for March 2015 and beyond

Thank You

The DBE Development Team

SAO/CfA
- Jonathan Weintroub
- Rurik Primiani
- Laura Vertatschitsch
- John Test
- Lindy Blackburn
- Katherine Rosenfeld

Westford Radio Telescope
- Mike Poirier
- Alex Burns

GGAO
- Katherine Pazamickas
- Jay Redmond

U of Arizona
- Dan Marrone
- Junhan Kim

MIT Haystack
- Russ McWhirter
- Geoff Crew
- Jason SooHoo
- Chris Beaudoin
- Chris Eckert
- Mike Titus
- Chet Ruszczyk
- Shep Doeleman
- Roger Cappallo
- Alan Rogers
- Arthur Niell
- Mike Hecht
- Colin Lonsdale
- Don Souza
- Pete Bollis

CASPER

XILINX®

HAYSTACK OBSERVATORY

The EHT wiki has been an important tool in the documentation and collaboration of this project.