Title: Scalable quantum computer architecture for superconducting flux qubits

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Abstract:

IQC Institute *for* Quantum Computing

University of Waterloo

Long-range coupling mechanism and architecture for superconducting flux qubits

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cond-mat/0702620

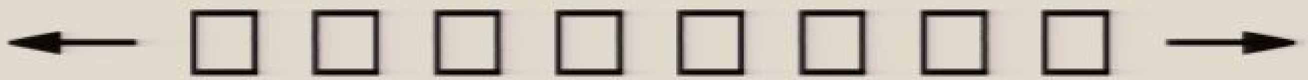
CENTRE FOR QUANTUM COMPUTER TECHNOLOGY ARC ARDA NSERC CRSNG

Overview

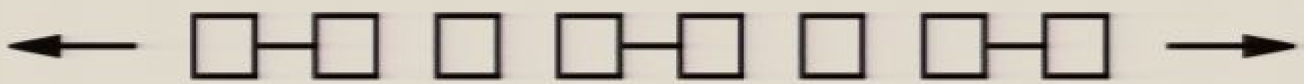
- What is scalability?
- Coupling flux qubits
- Why long-range coupling?
- Long-range coupling of flux qubits
- Interlude: error correction
- Universal set of gates
- Designing the flux qubit coupler network
- Calculating thresholds
- Conclusion and further work

Scalability

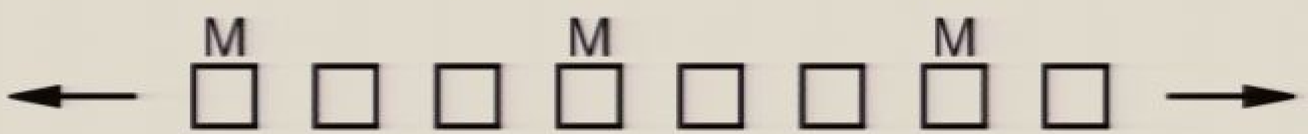
- Arbitrarily large number of qubits



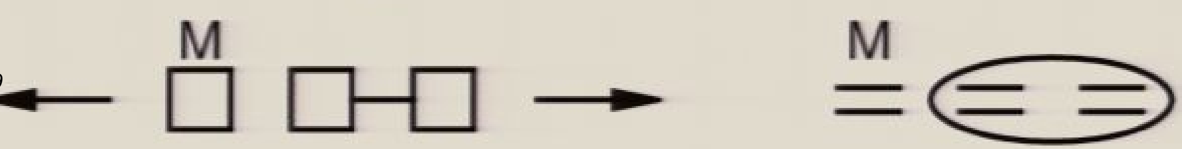
- Number of simultaneous gates proportional to number of qubits



- Number of simultaneous measurements proportional to number of qubits

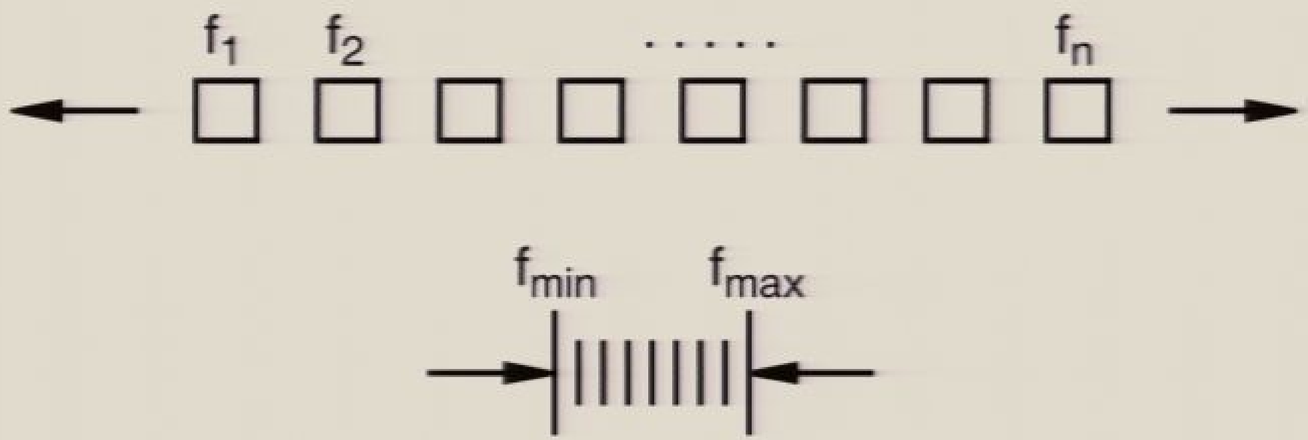


- Physics of gates and measurements independent of number of qubits

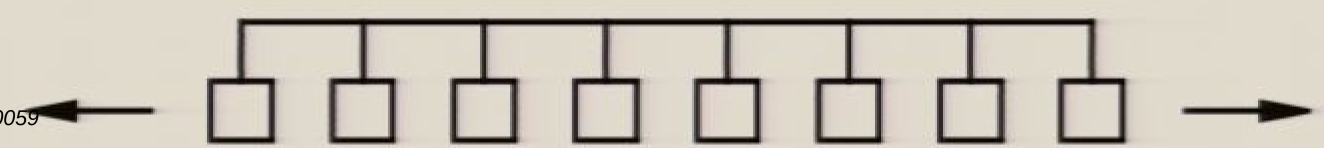


Common unscalable examples

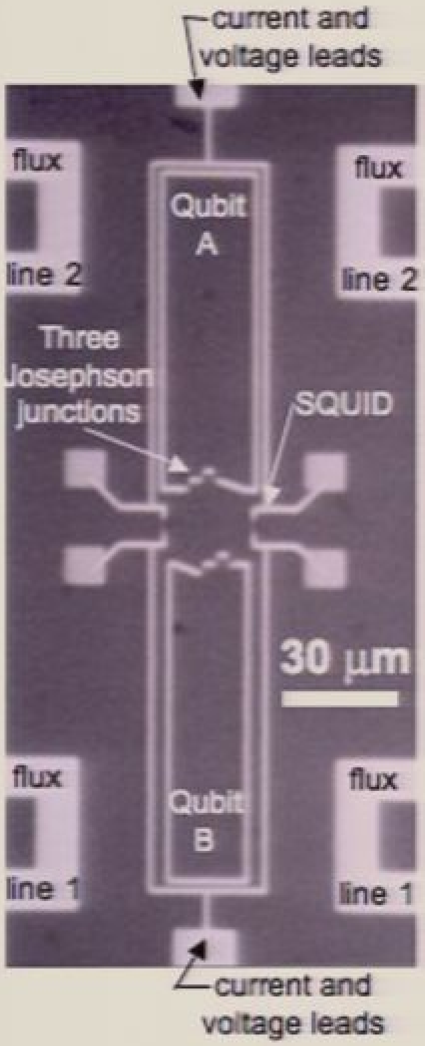
- Anything with frequency crowding

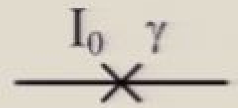


- Anything with a single shared device for gates or measurement

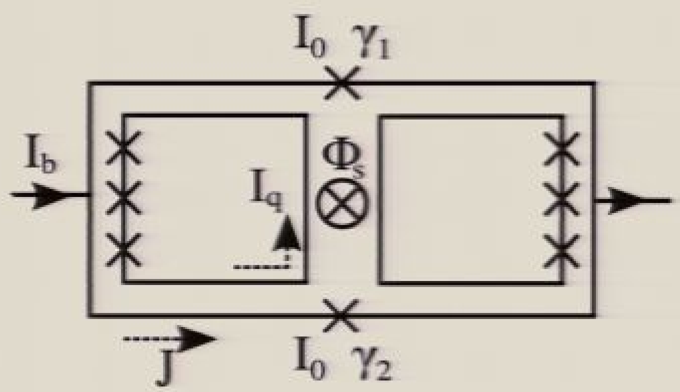


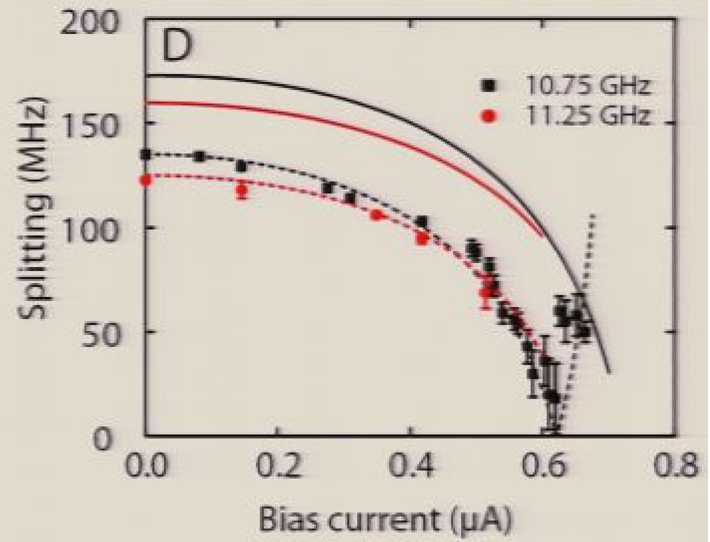
Our starting point



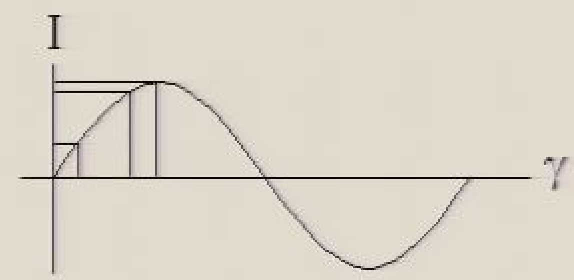


$$I = I_0 \sin\gamma$$





- $I_b = I_0 \sin\gamma_1 + I_0 \sin\gamma_2$
- $2J = I_0 \sin\gamma_2 - I_0 \sin\gamma_1$
- $\gamma_1 - \gamma_2 + \frac{2\pi}{\Phi_0}(\Phi_s - LJ) = 0$



Theory: B. L. T. Plourde et al., PRB 70, 140501(R) (2004), UC Berkeley

Shortcomings

- Need long-range interactions
- Thresholds
  - unlimited range, unlimited qubits: ~ 10^{-2}

    Knill, quant-ph/0410199
  - unlimited range, many qubits: ~ 10^{-3}–10^{-4}

    Steane, Phys. Rev. A 68, 042322 (2003)
  - 2D lattice, nearest neighbor: ~ 10^{-5}

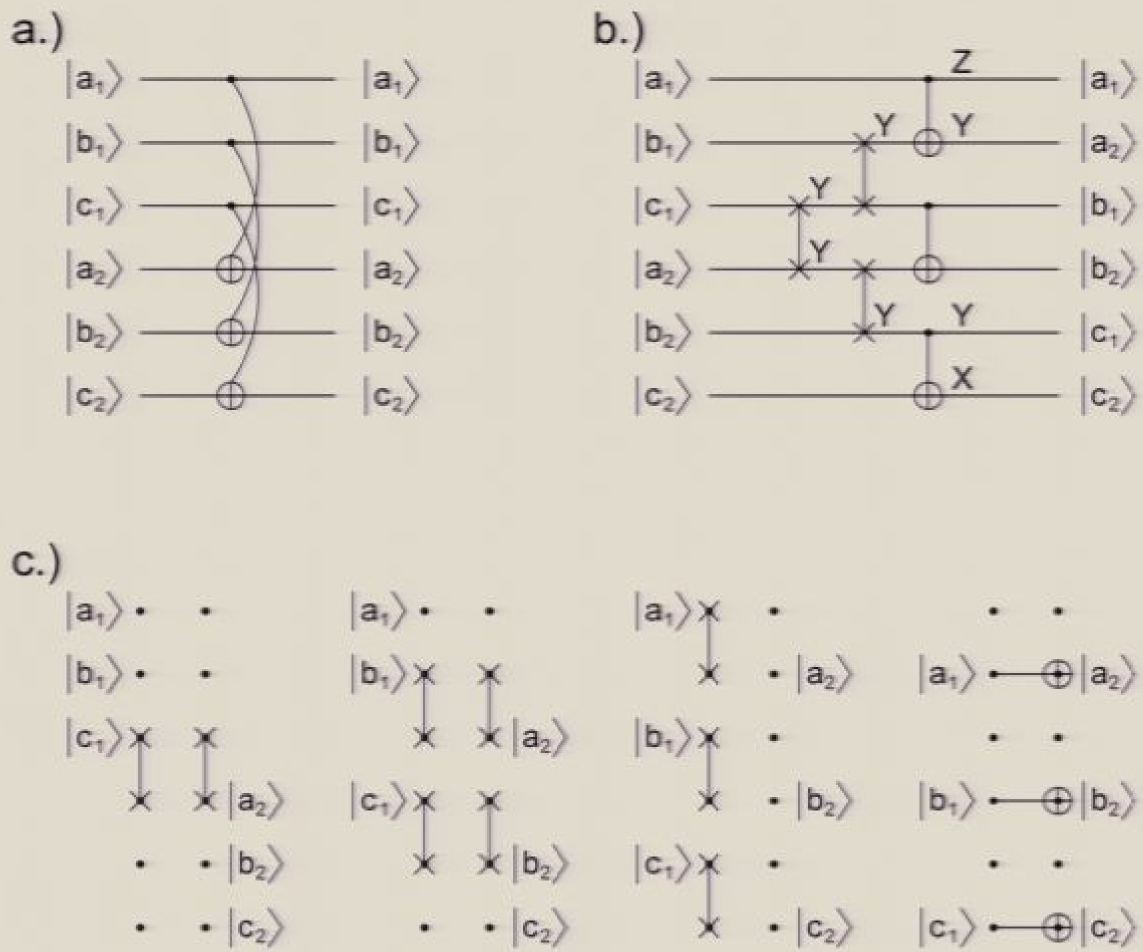
    Svore, QIC 7, 297 (2007)
  - bilinear nearest neighbor: ~ 10^{-6}

    Stephens, quant-ph/0702201
  - linear nearest neighbor: ~ 10^{-8}

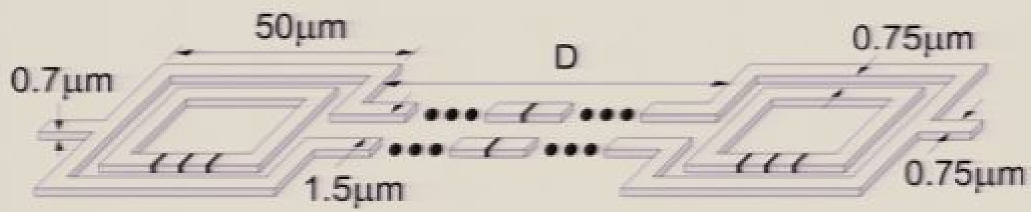
    Stephens, in preparation

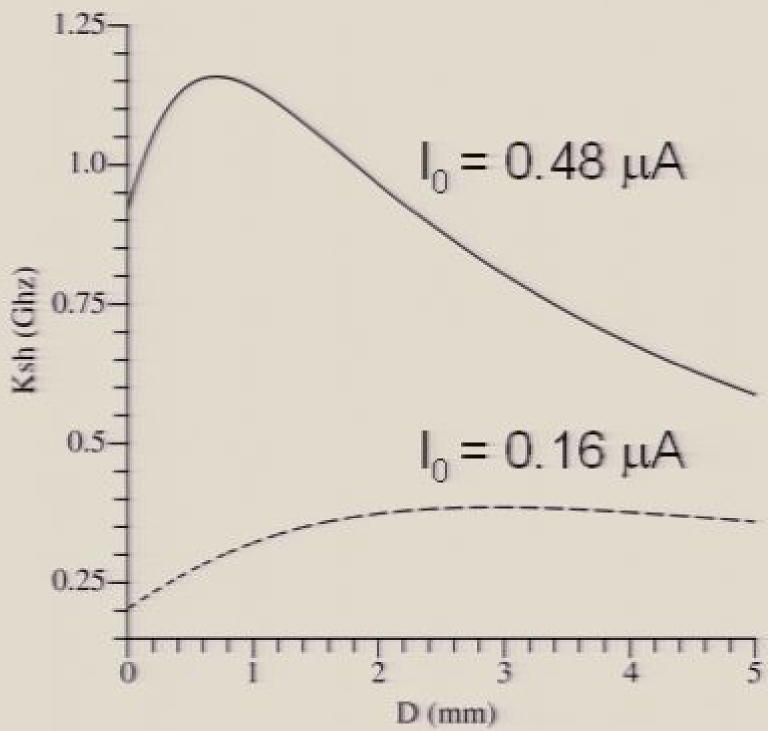
Why long-range coupling?

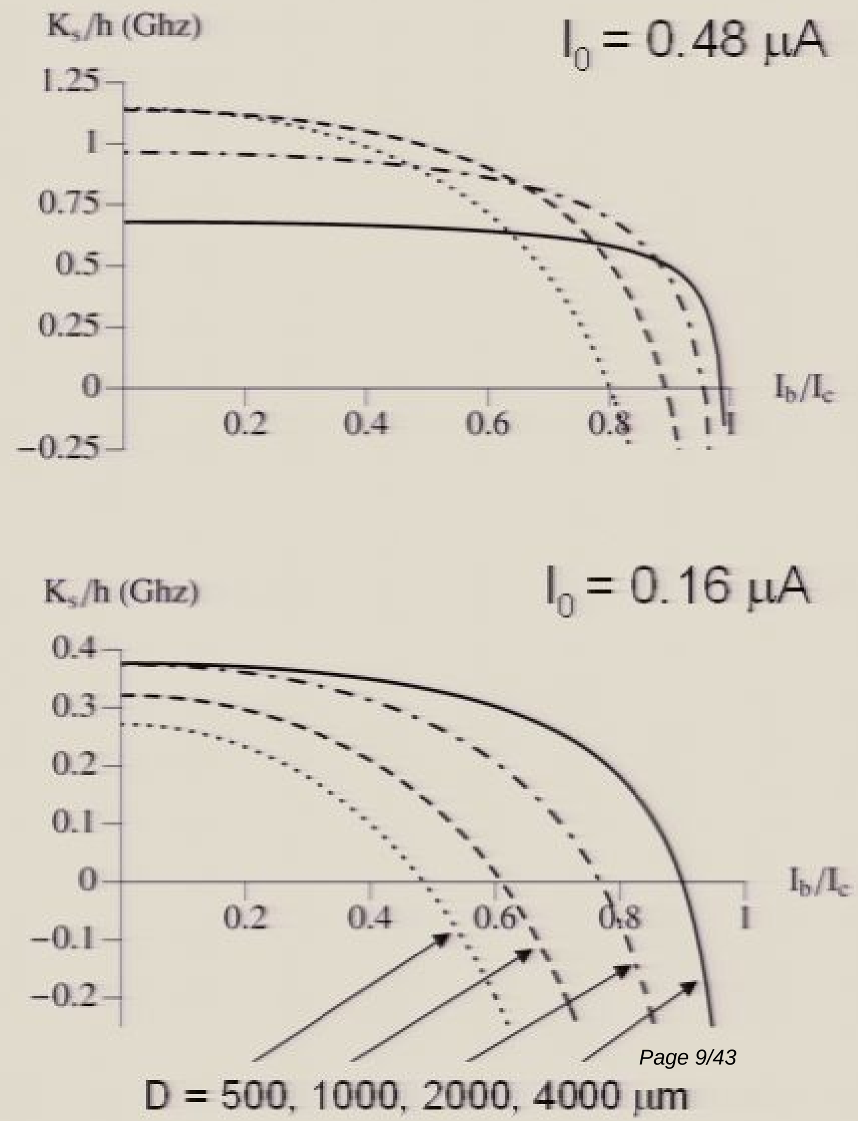
- Case a.)
  - qubits: 2n
  - gates: n
  - idle: 0
  - depth: 1
- Case c.)
  - qubits: 4n
  - gates: $2n^2 + n$
  - idle: $2n^2$
  - depth: $2n + 1$



Extending the coupler

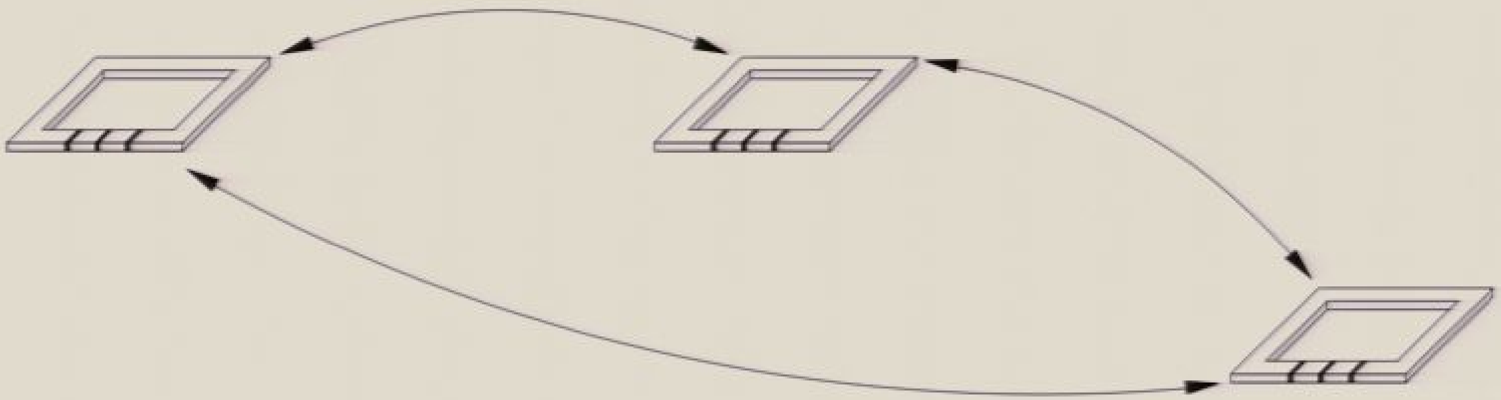


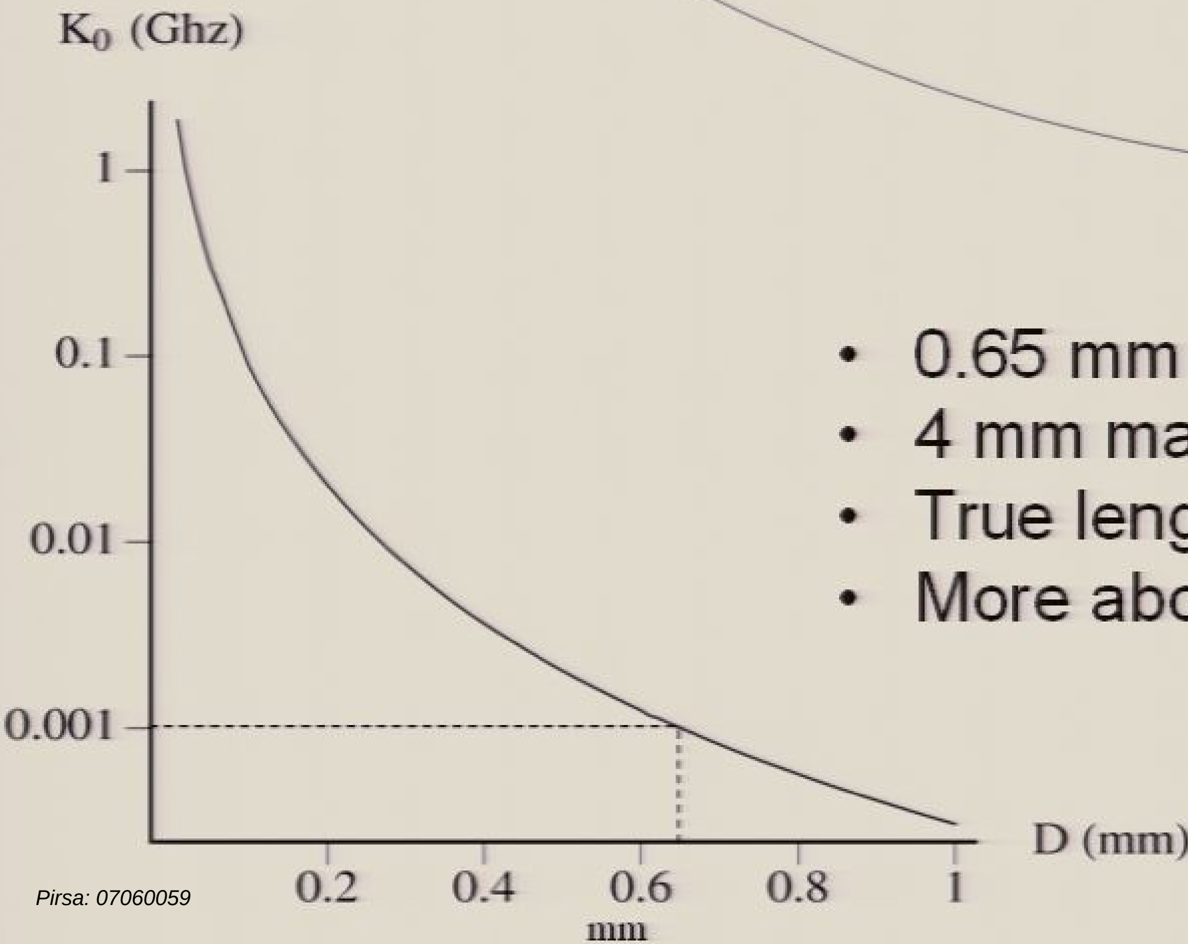




Fowler et al., cond-mat/0702620

True coupler length: crosstalk

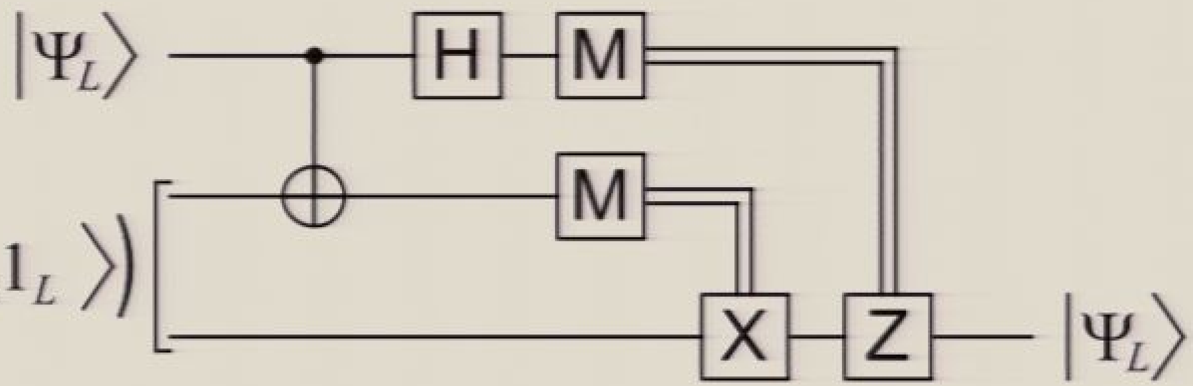




- 0.65 mm minimum separation
- 4 mm maximum separation
- True length: 5-6 qubits
- More about this later...

Interlude: error correction

- Knill



$$|0_L\rangle = \frac{1}{\sqrt{8}}(|0000000\rangle + |1010101\rangle + |0110011\rangle + |1100110\rangle + |0001111\rangle + |1011010\rangle + |0111100\rangle + |1101001\rangle)$$

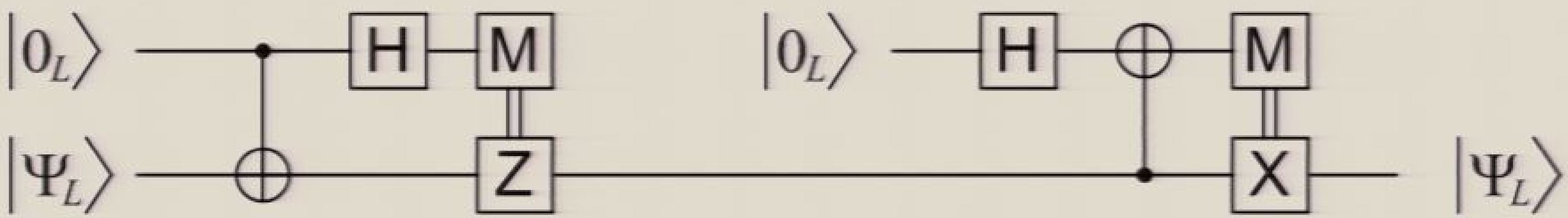
$$|1_L\rangle = \frac{1}{\sqrt{8}}(|1111111\rangle + |0101010\rangle + |1001100\rangle + |0011001\rangle + |1110000\rangle + |0100101\rangle + |1000011\rangle + |0010110\rangle)$$

- Best approach for high threshold ~ 10^{-2}

Knill, quant-ph/0410199

Interlude: error correction

- Steane: threshold ~ 10^{-3} to 10^{-4}

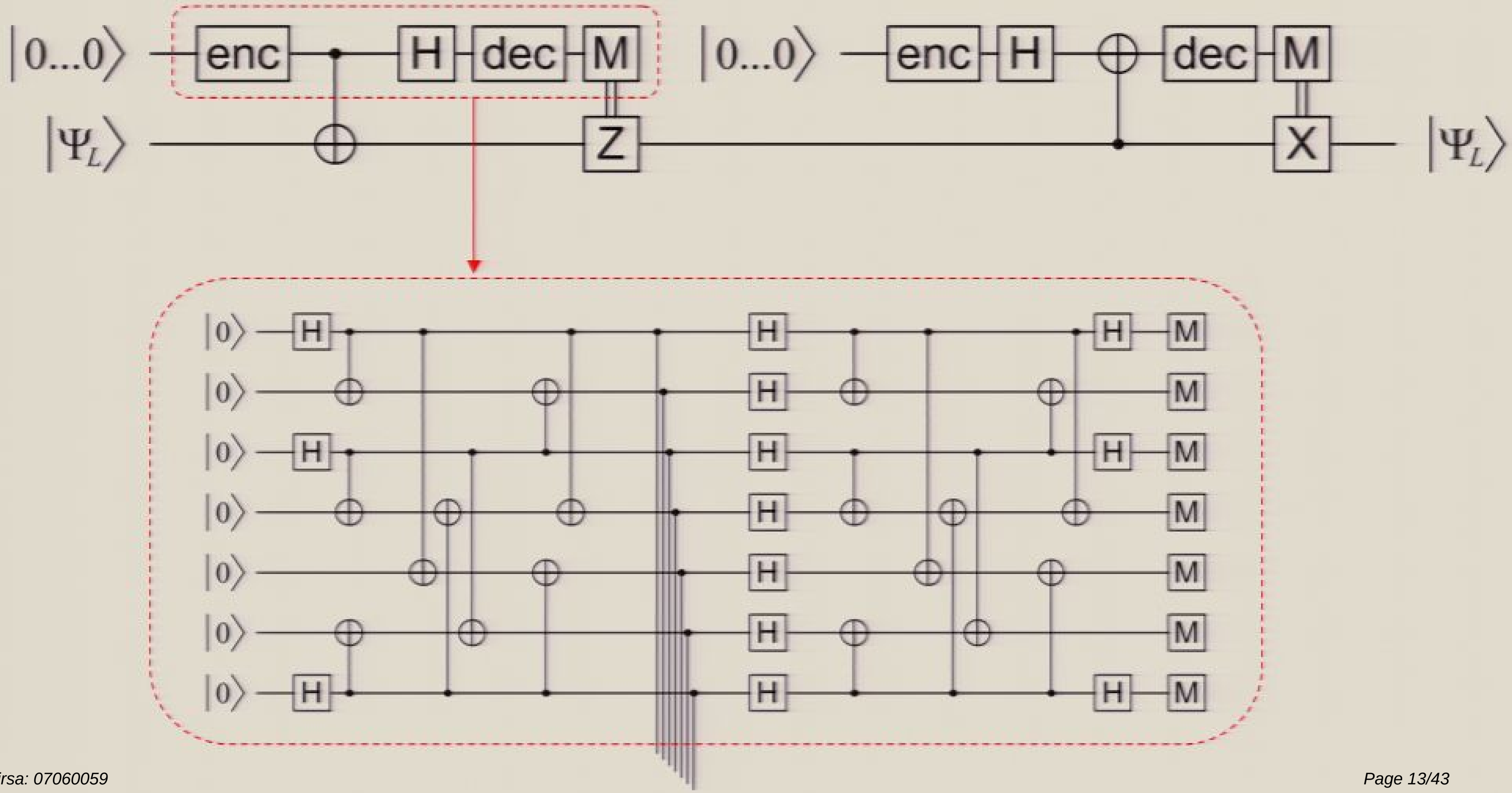


- Still need to repeat logical state preparation
- Still need to repeat measurements
- Still need large ancilla factories
- Still need very long-range interactions

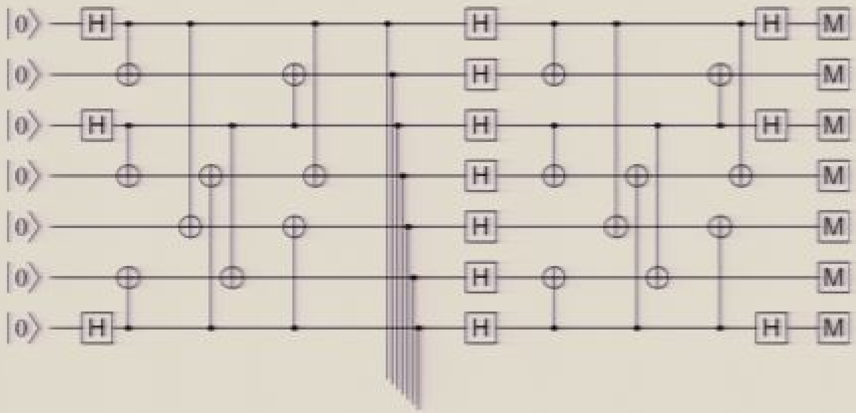
Steane, Phys. Rev. A 68, 042322 (2003)

Interlude: error correction

- Steane/DiVincenzo PRL 98, 020501 (2007)

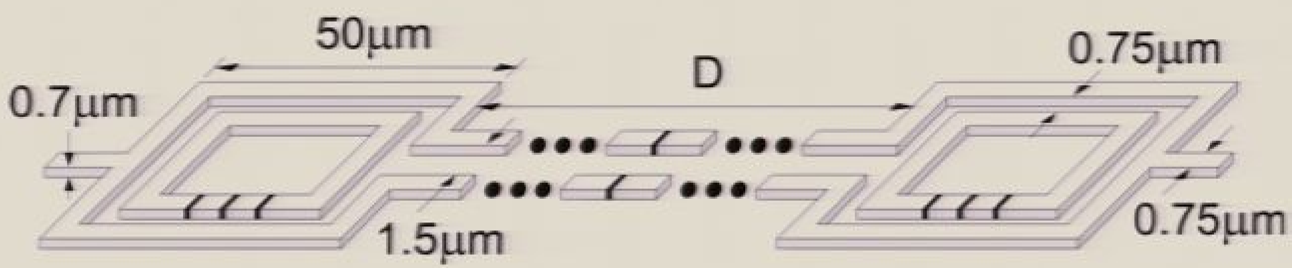


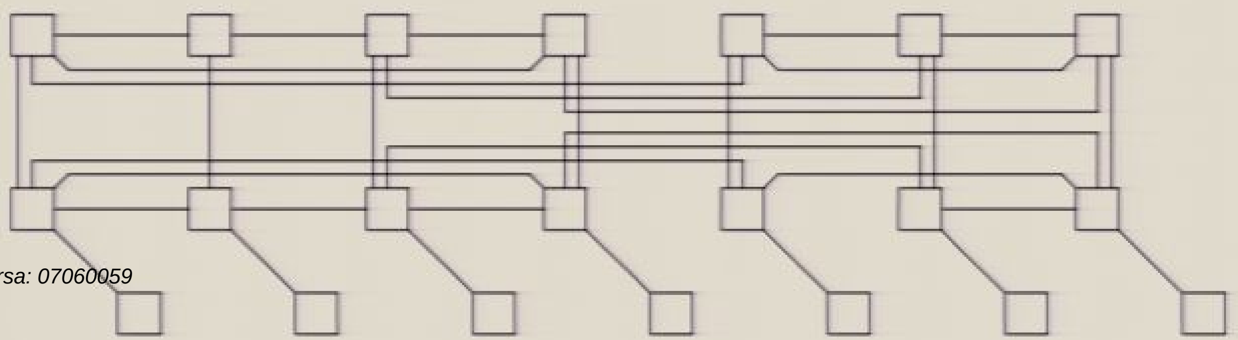
Laying out the circuitry



- Error correction

- Coupler

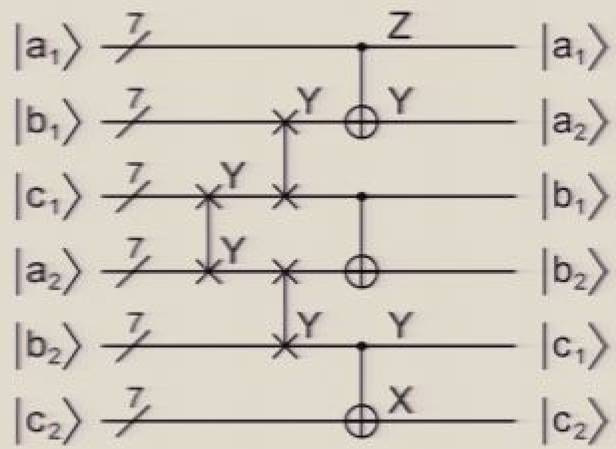


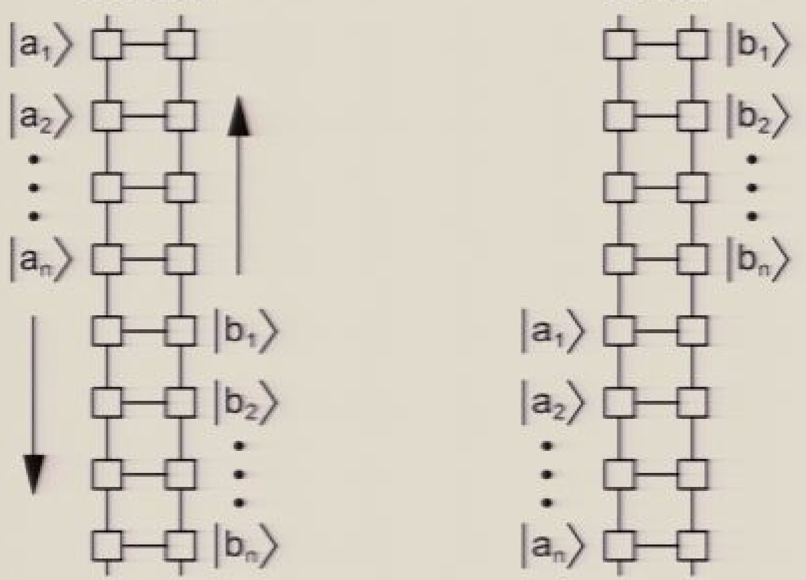


- Network

Level 2 circuitry

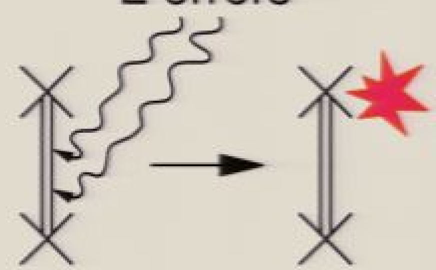
- Must still avoid linear nearest neighbor





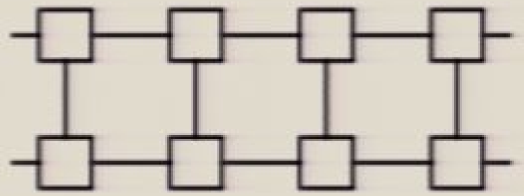
after n^2 swaps

- Need logical bilinear network
- Permits fault-tolerant swap

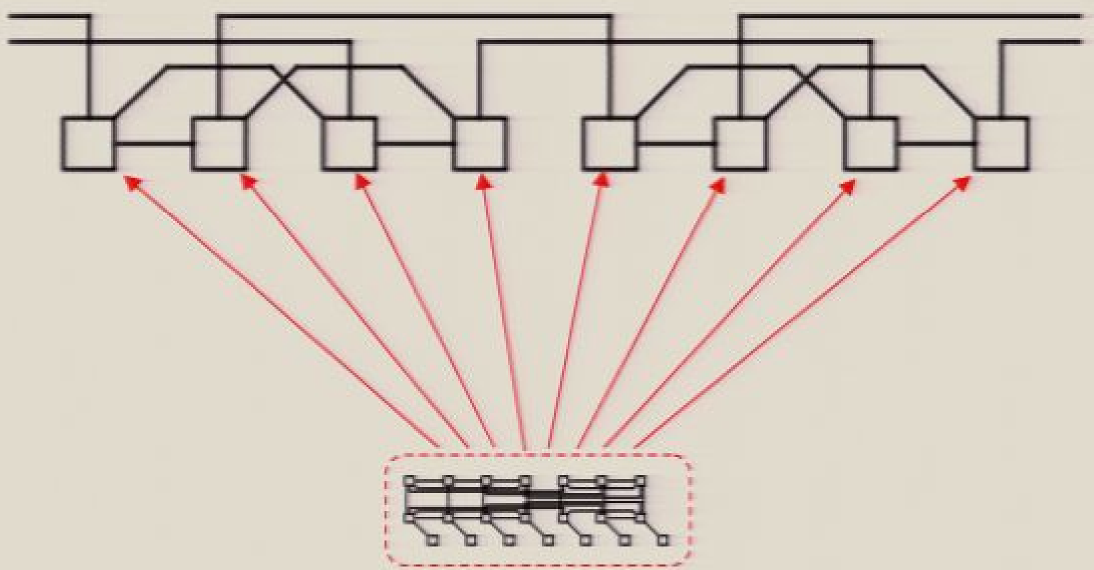


Level 2 circuitry

- Can't do logical bilinear directly

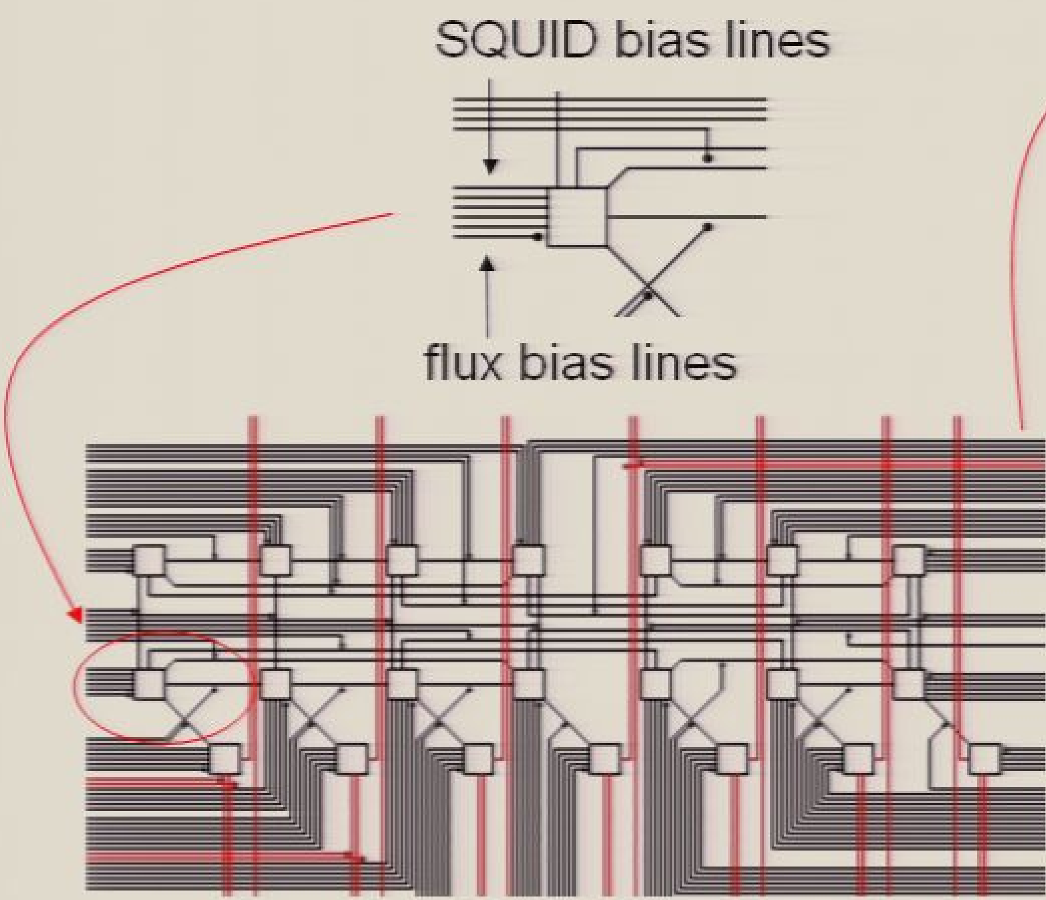


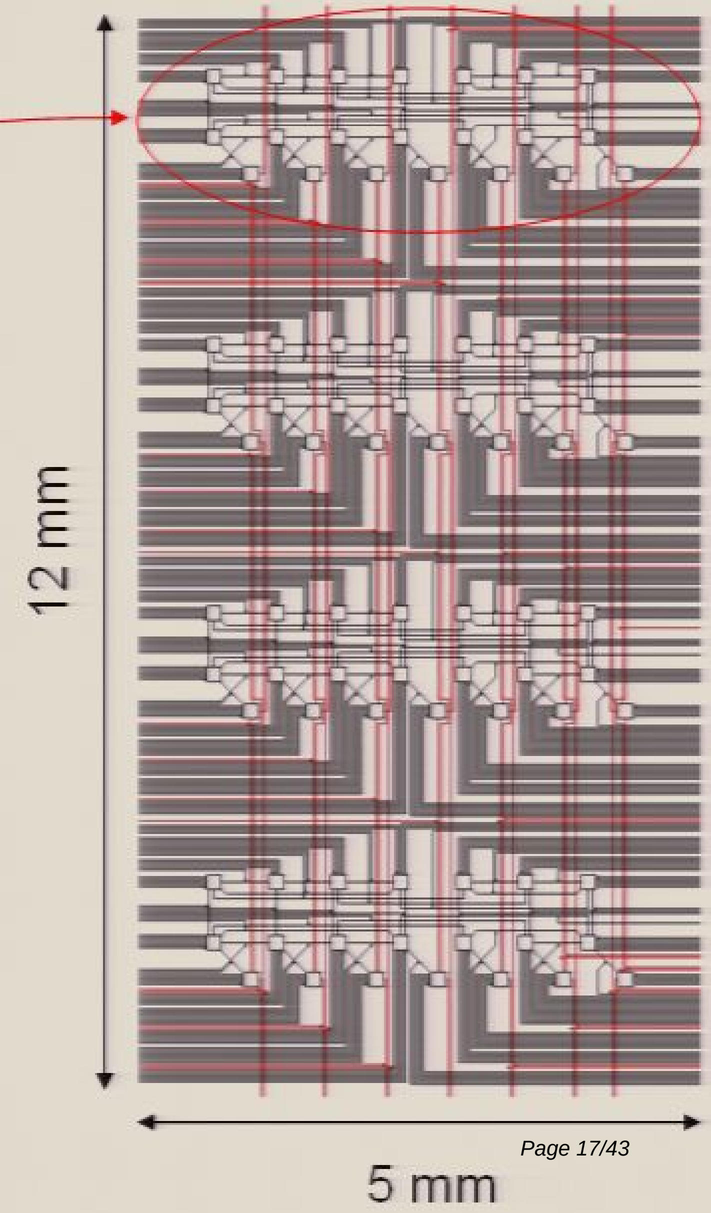
- Need to stretch the design



Level 2 circuitry

- Must control each qubit

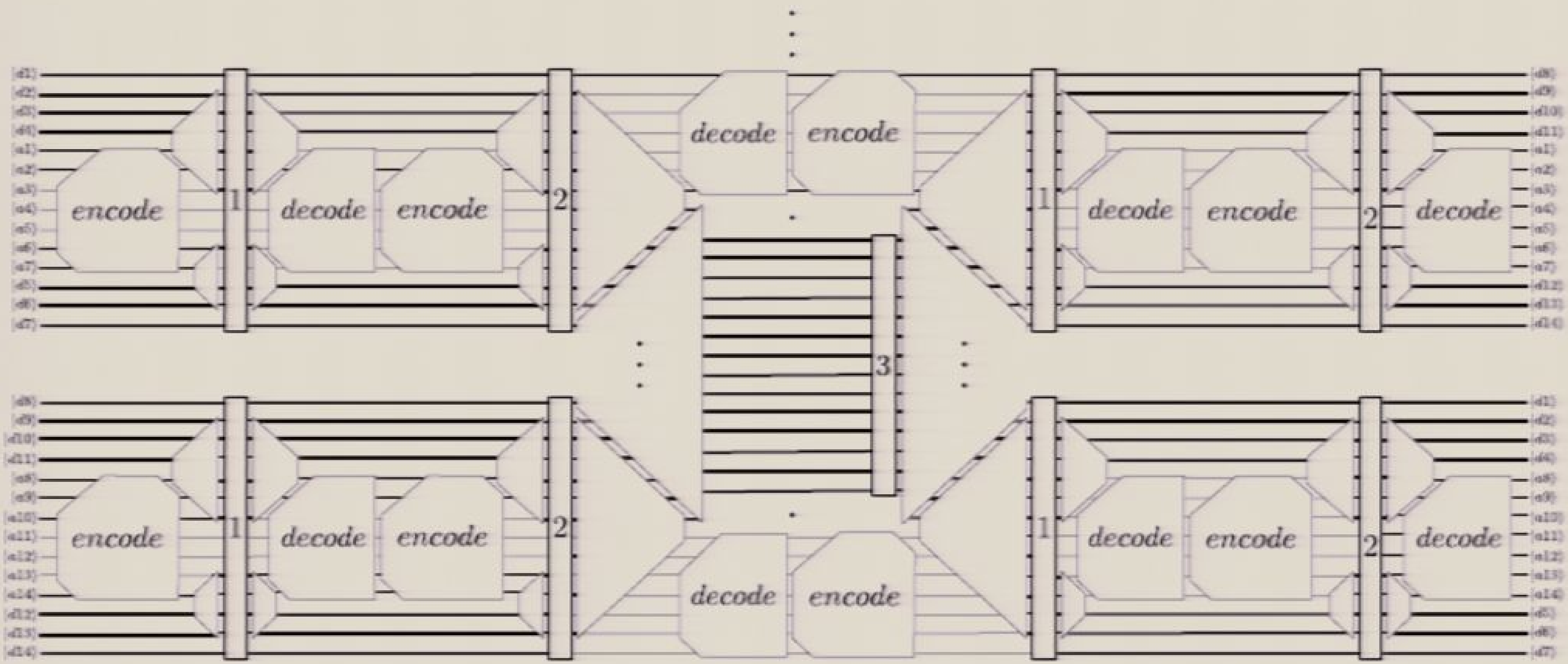




- 1 wire per 40 μm
- Fowler et al., cond-mat/0702620

Level 3 circuitry

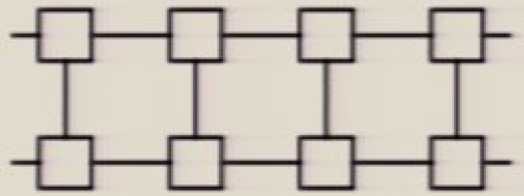
- Linear nearest neighbor with fault-tolerant swap



- Each horizontal line represents 2×21^2 qubits

Level 2 circuitry

- Can't do logical bilinear directly



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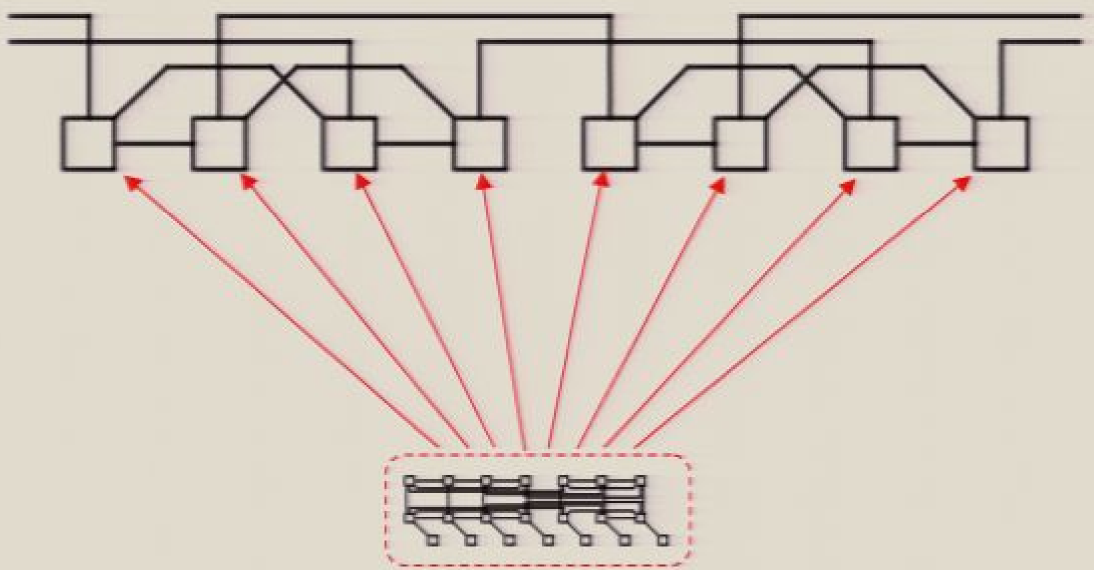
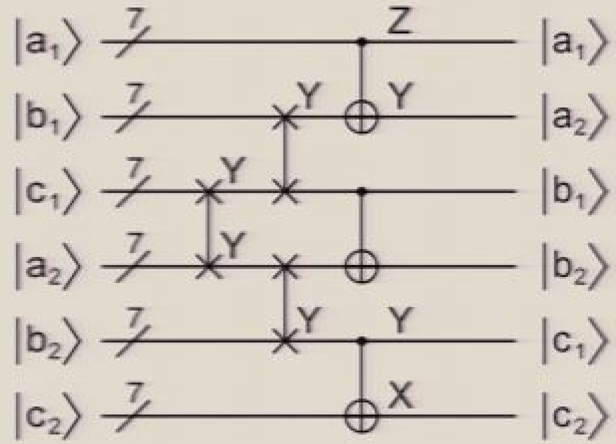


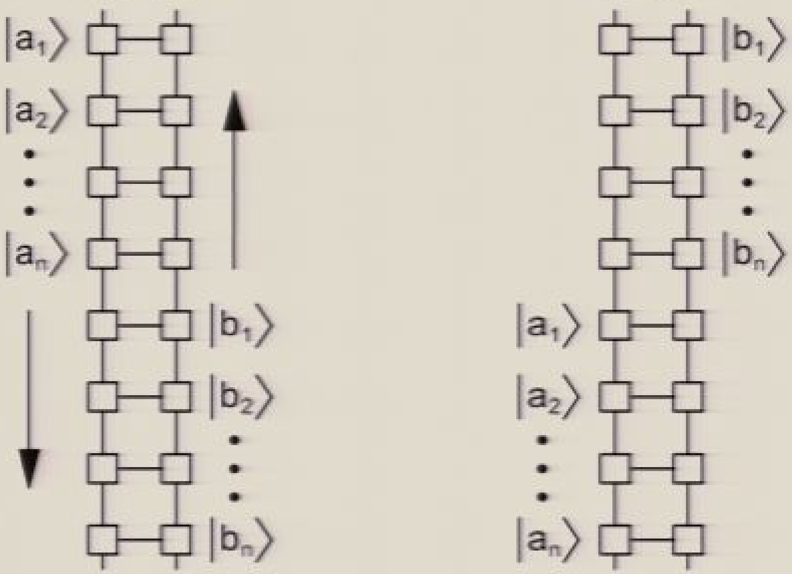
Level 2 circuitry

- Must still avoid linear nearest neighbor



initial

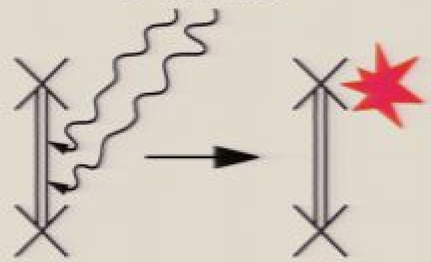
final



after n^2 swaps

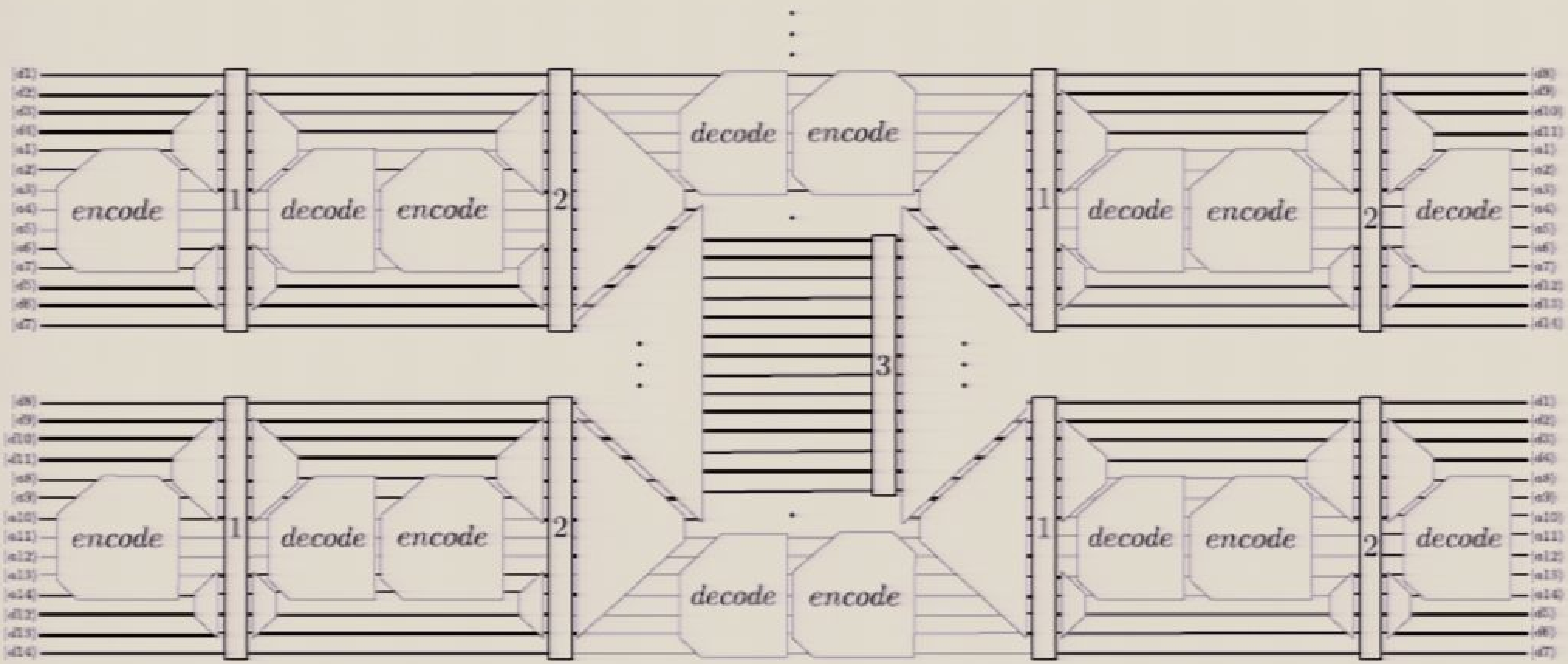
- Need logical bilinear network
- Permits fault-tolerant swap

2 errors



Level 3 circuitry

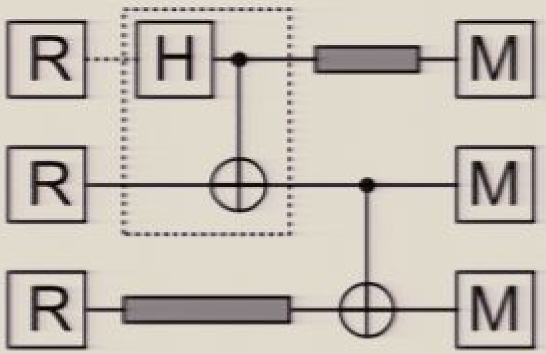
- Linear nearest neighbor with fault-tolerant swap



- Each horizontal line represents $2x21^2$ qubits

Calculating thresholds

- Random example pretending to cope with one error

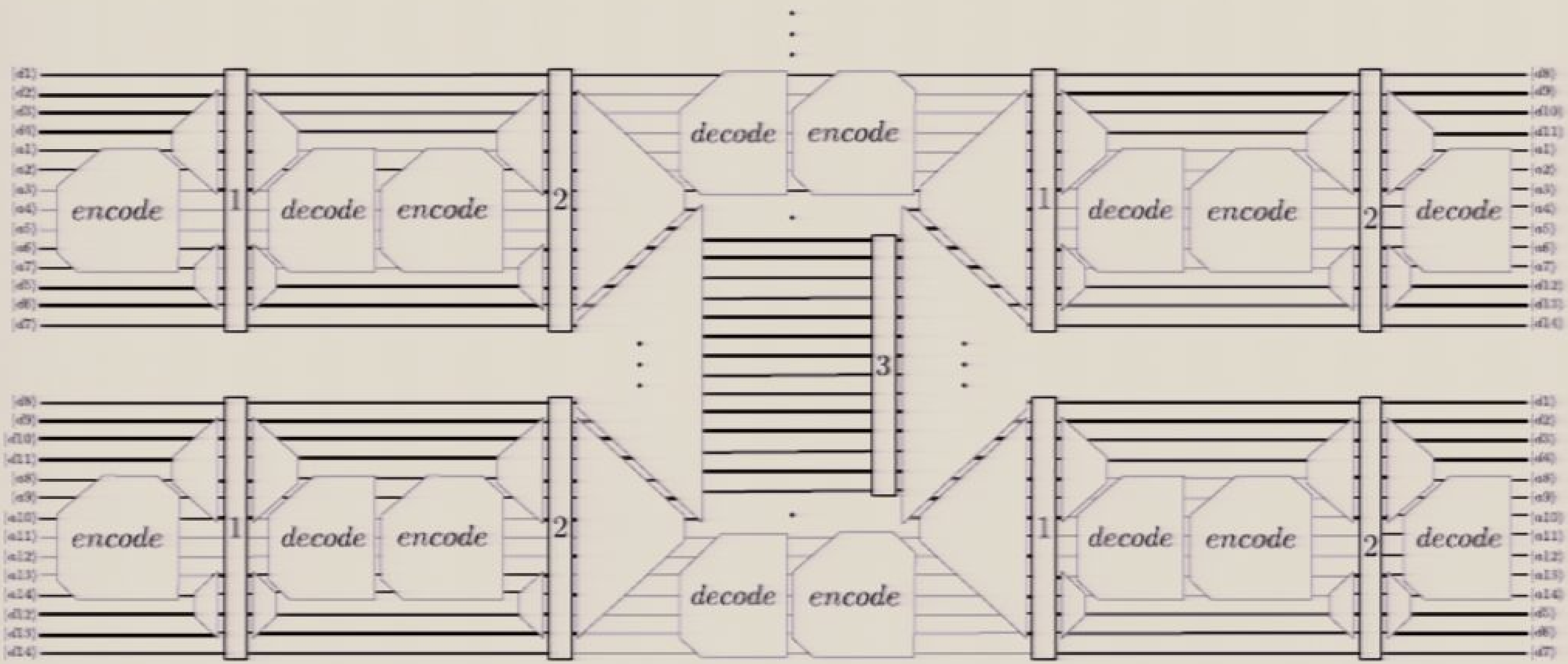


- Resets: 3
- Gates: 2
- Waits: 2
- Measurements: 3

$$
\begin{aligned}
p_{fail} &= 1 - p_{success} \\
&= 1 - (1-p_{reset})^3(1-p_{gate})^2(1-p_{wait})^2(1-p_{meas})^3 \\
&\quad - p_{reset}(1-p_{reset})^2(1-p_{gate})^2(1-p_{wait})^2(1-p_{meas})^3 \\
&\quad - p_{gate}(1-p_{reset})^3(1-p_{gate})(1-p_{wait})^2(1-p_{meas})^3 \\
&\quad - p_{wait}(1-p_{reset})^3(1-p_{gate})^2(1-p_{wait})(1-p_{meas})^3 \\
&\quad - p_{meas}(1-p_{reset})^3(1-p_{gate})^2(1-p_{wait})^2(1-p_{meas})^2
\end{aligned}
$$

Level 3 circuitry

- Linear nearest neighbor with fault-tolerant swap



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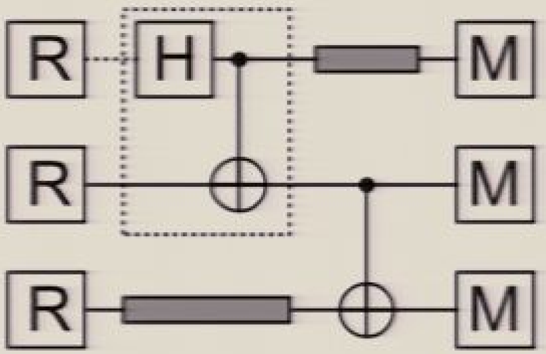


- Resets: 3
- Gates: 2
- Waits: 2
- Measurements: 3

$$p_{fail} = 1 - p_{success}$$

$$= 1 - (1 - p_{reset})^3 (1 - p_{gate})^2 (1 - p_{wait})^2 (1 - p_{meas})^3$$

$$- p_{reset} (1 - p_{reset})^2 (1 - p_{gate})^2 (1 - p_{wait})^2 (1 - p_{meas})^3$$

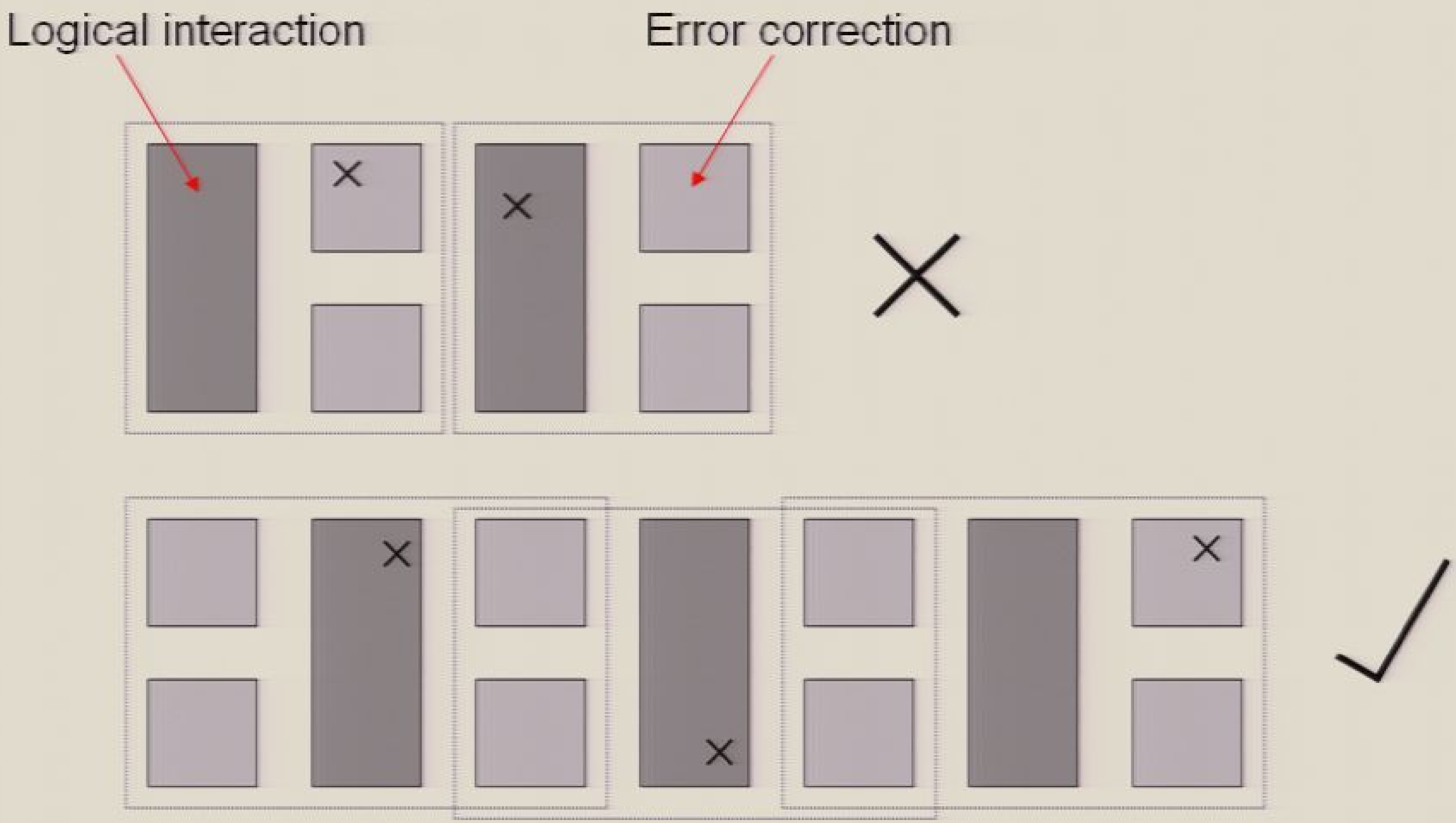
$$- p_{gate} (1 - p_{reset})^3 (1 - p_{gate})(1 - p_{wait})^2 (1 - p_{meas})^3$$

$$- p_{wait} (1 - p_{reset})^3 (1 - p_{gate})^2 (1 - p_{wait})(1 - p_{meas})^3$$

$$- p_{meas} (1 - p_{reset})^3 (1 - p_{gate})^2 (1 - p_{wait})^2 (1 - p_{meas})^2$$

Extended rectangles

- How much circuitry needs to be included?



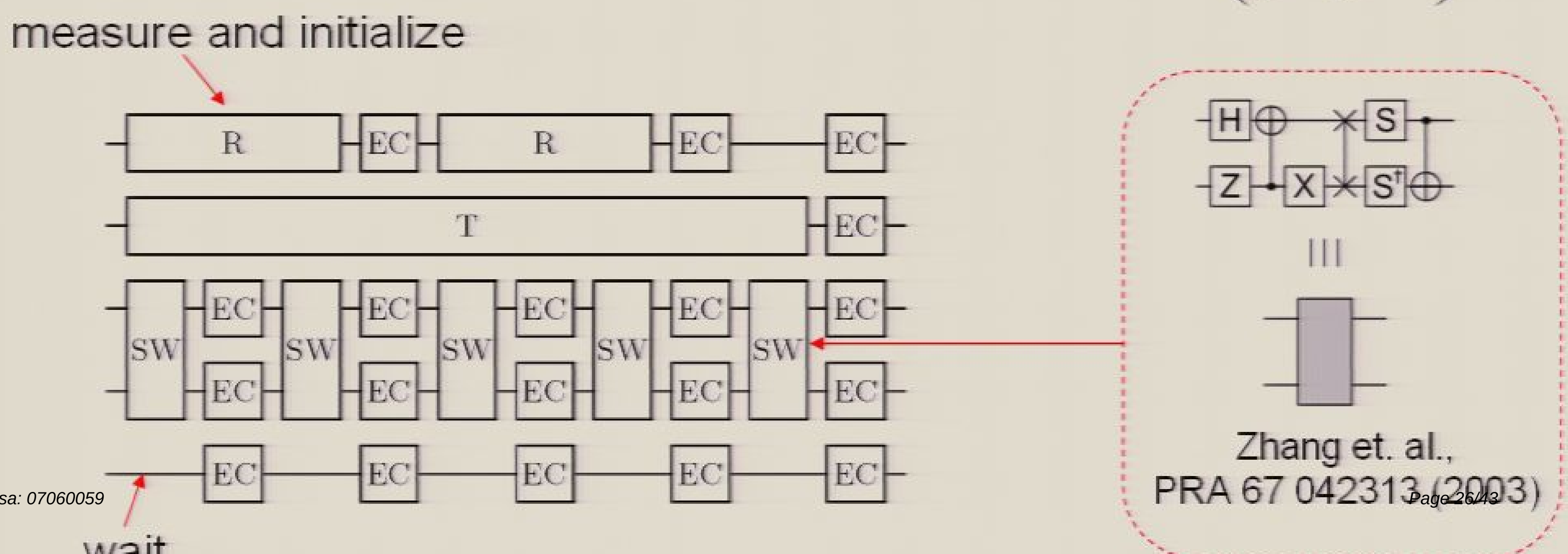
Panos Aliferis, Daniel Gottesman and John Preskill, quant-ph/0504218

Which threshold?

- Must calculate threshold of most complex gate
- Universal gate set:
  - H, X, Z, S, $S^\dagger$, and all combinations (23)
  - CNOT, SWAP
  - Measure, initialize, wait
  - T-gate (π/8-gate)

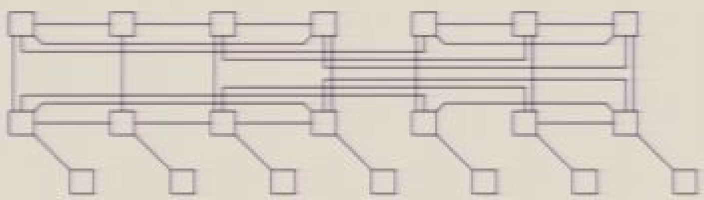
$$S = \begin{pmatrix} 1 & 0 \\ 0 & i \end{pmatrix}$$

$$T = \begin{pmatrix} 1 & 0 \\ 0 & e^{i\pi/4} \end{pmatrix}$$



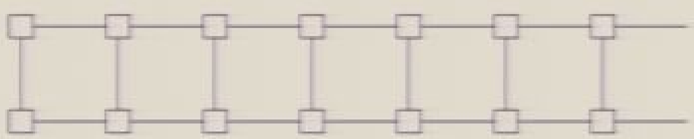
Three universal gate sets

- Non-local network



	$i=m$	$i=S$	$i=r$	depth
$j=m$	$206+28t_r$	100	28	$15+2t_r$
$j=S$	$398+56t_r$	207	56	$15+2t_r$
$j=T$	$1067+133t_r$	289	98	$75+10t_r$
$j=r$	$366+42t_r$	125	42	$30+4t_r$

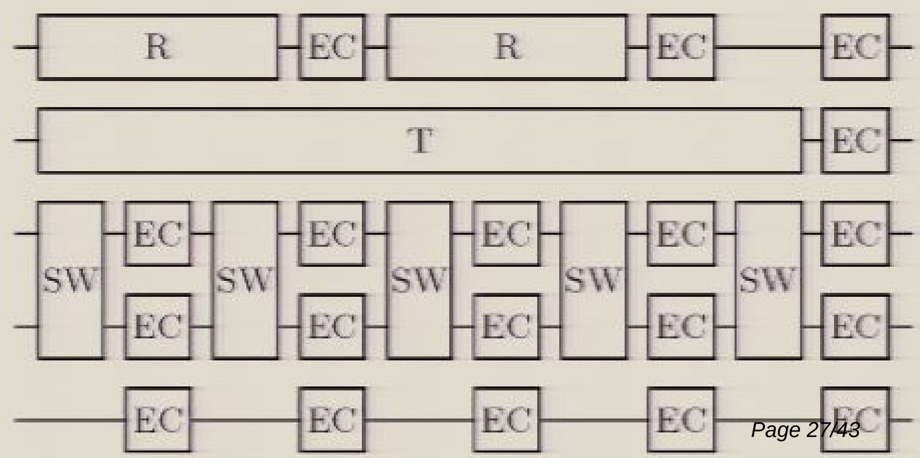
- Bilinear network



	$i=m$	$i=S$	$i=T$	$i=r$	depth
$j=m$	710	408	0	40	45
$j=S$	1114	1122	0	80	45
$j=T$	3171	1330	28	137	225
$j=r$	1129	510	0	57	90

- Linear nearest neighbor

	$i=m$	$i=S$	$i=T$	$i=r$	depth
$j=m$	558	204	0	28	38
$j=S$	824	603	0	56	38
$j=T$	2496	670	28	98	190
$j=r$	974	255	0	42	76



Thresholds for the architecture

- Four variables: p_{swap}, p_{memory}, $p_{readout}$, $t_{readout}$
- Set: $p_{memory} = 0.1p_{swap}$, $p_{readout} = p_{swap}$, $t_{readout} = 10$

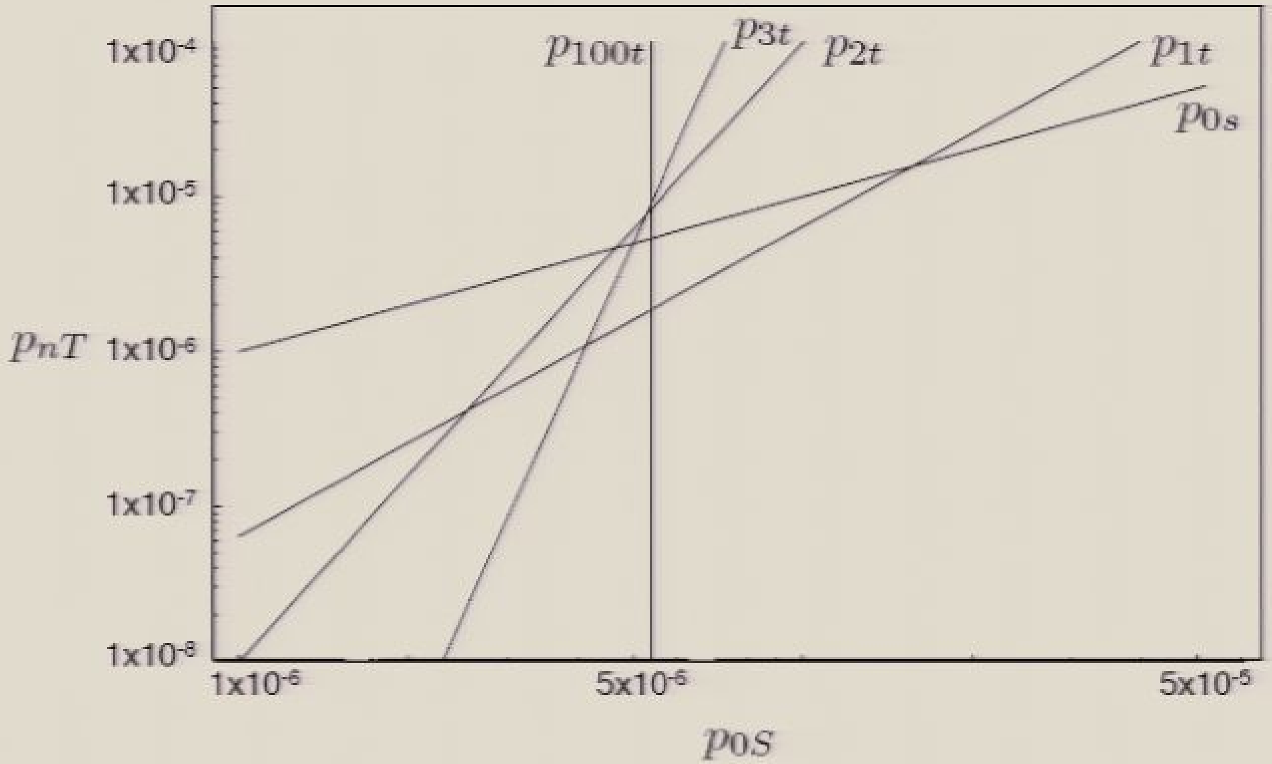
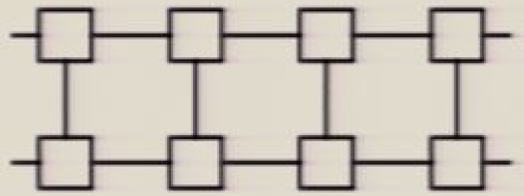


FIG. 1: p_{0S} and $p_{nT}(p_{0S}, 0.1, 1.0, 10.0)$ for $n = \{1, 2, 3, 100\}$. The lower bound to the 100 T threshold is 5.36×10^{-6}.

- Infinite level threshold: ~5×10^{-6}, level-1 threshold ~10^{-5}

Level 2 circuitry

- Can't do logical bilinear directly



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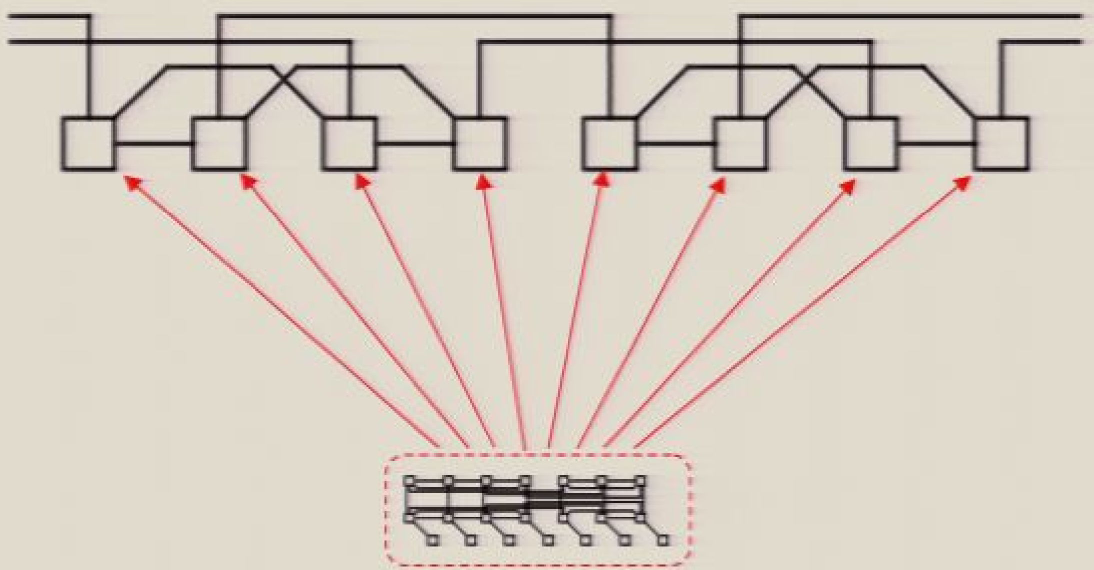
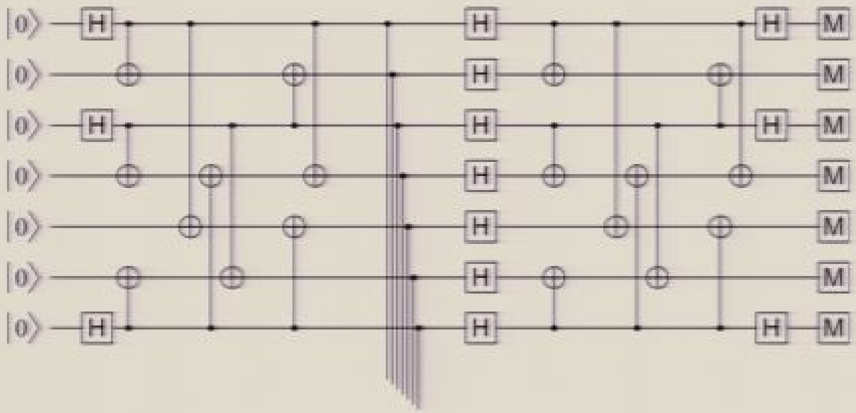
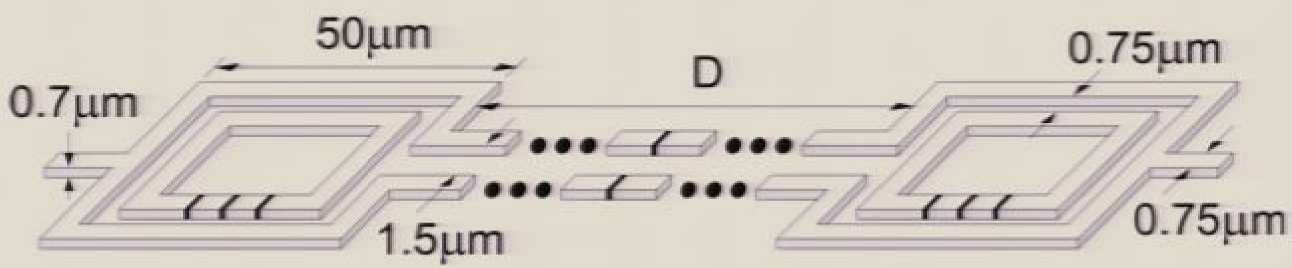


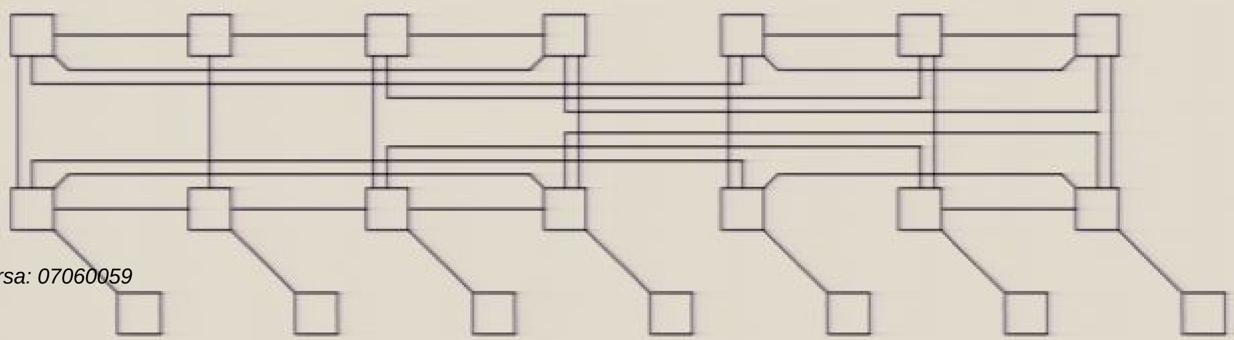
Laying out the circuitry



- Error correction

- Coupler





- Network

Three universal gate sets

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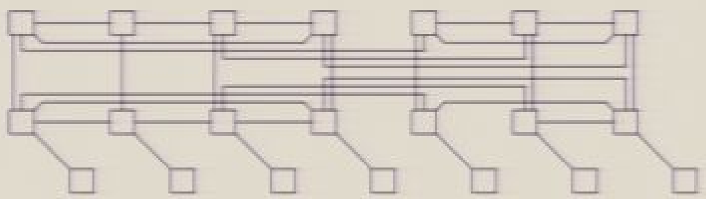

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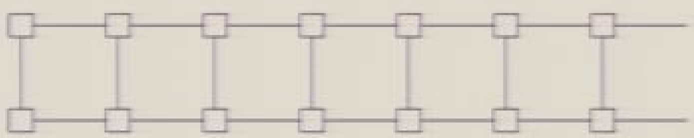
$j=S$	$398+56t_r$	207	56	$15+2t_r$
$j=T$	$1067+133t_r$	289	98	$75+10t_r$
$j=r$	$366+42t_r$	125	42	$30+4t_r$

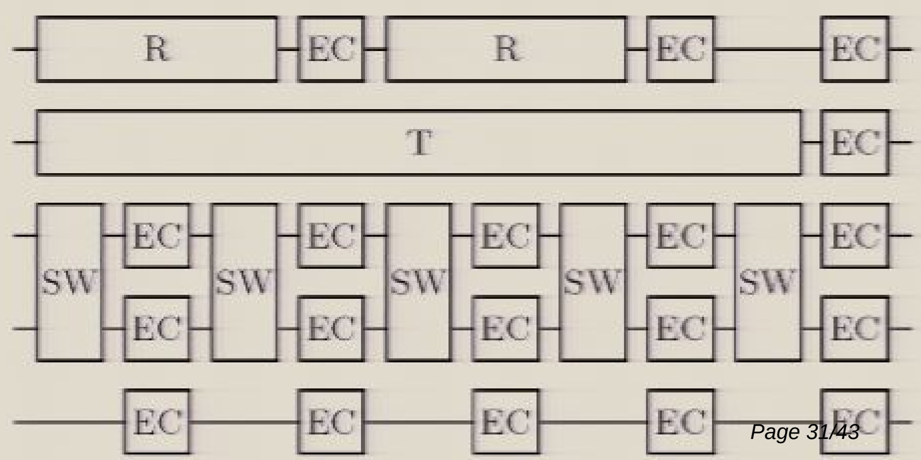
- Bilinear network



	$i=m$	$i=S$	$i=T$	$i=r$	depth
$j=m$	710	408	0	40	45
$j=S$	1114	1122	0	80	45
$j=T$	3171	1330	28	137	225
$j=r$	1129	510	0	57	90

- Linear nearest neighbor

	$i=m$	$i=S$	$i=T$	$i=r$	depth
$j=m$	558	204	0	28	38
$j=S$	824	603	0	56	38
$j=T$	2496	670	28	98	190
$j=r$	974	255	0	42	76



Thresholds for the architecture

- Four variables: p_{swap}, p_{memory}, $p_{readout}$, $t_{readout}$
- Set: $p_{memory} = 0.1p_{swap}$, $p_{readout} = p_{swap}$, $t_{readout} = 10$

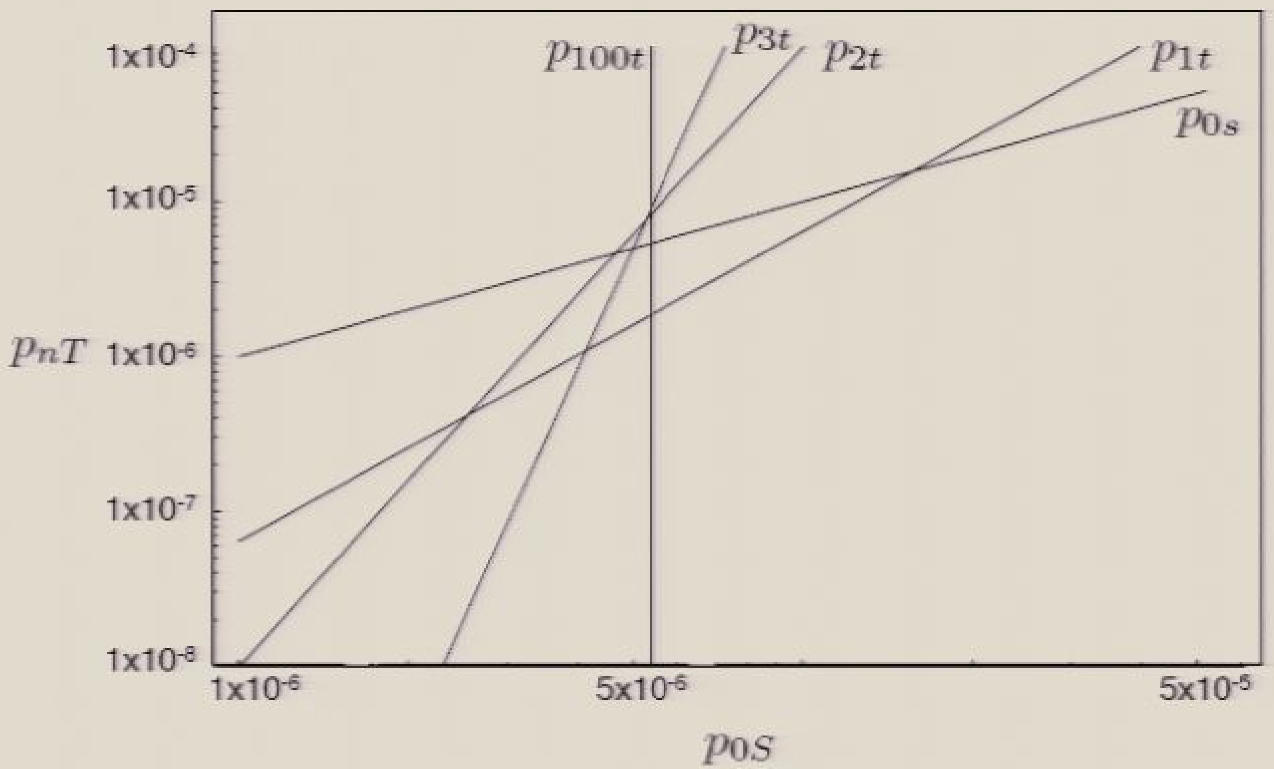
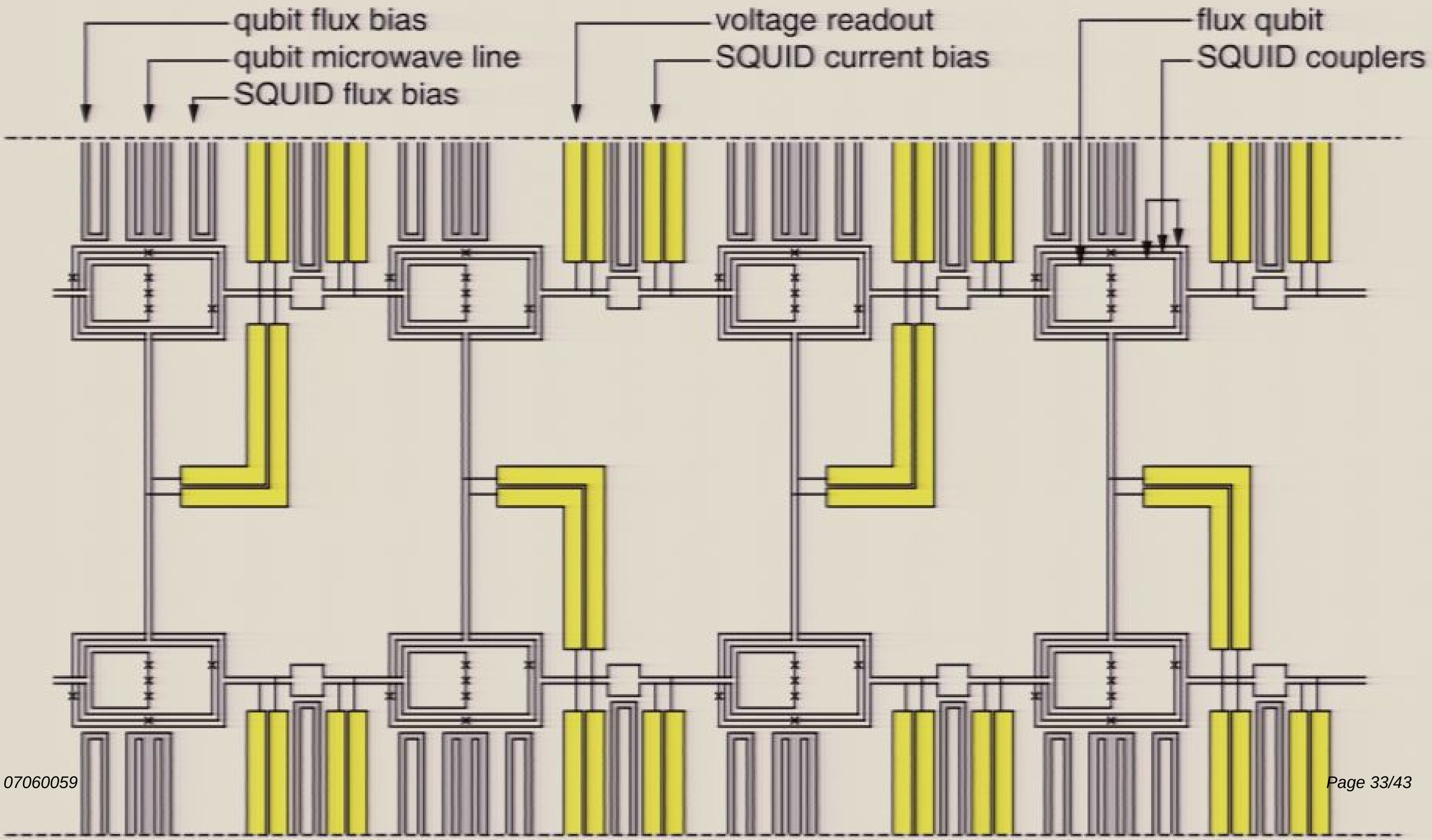


FIG. 1: p_{0S} and $p_{nT}(p_{0S}, 0.1, 1.0, 10.0)$ for $n = \{1, 2, 3, 100\}$. The lower bound to the 100 T threshold is 5.36×10^{-6}.

- Infinite level threshold: ~$5\text{x}10^{-6}$, level-1 threshold ~10^{-5}

Bilinear details

- Comparable threshold 2×10^{-6} (Stephens, quant-ph/0702201)
- Simpler construction likely to outweigh lower threshold



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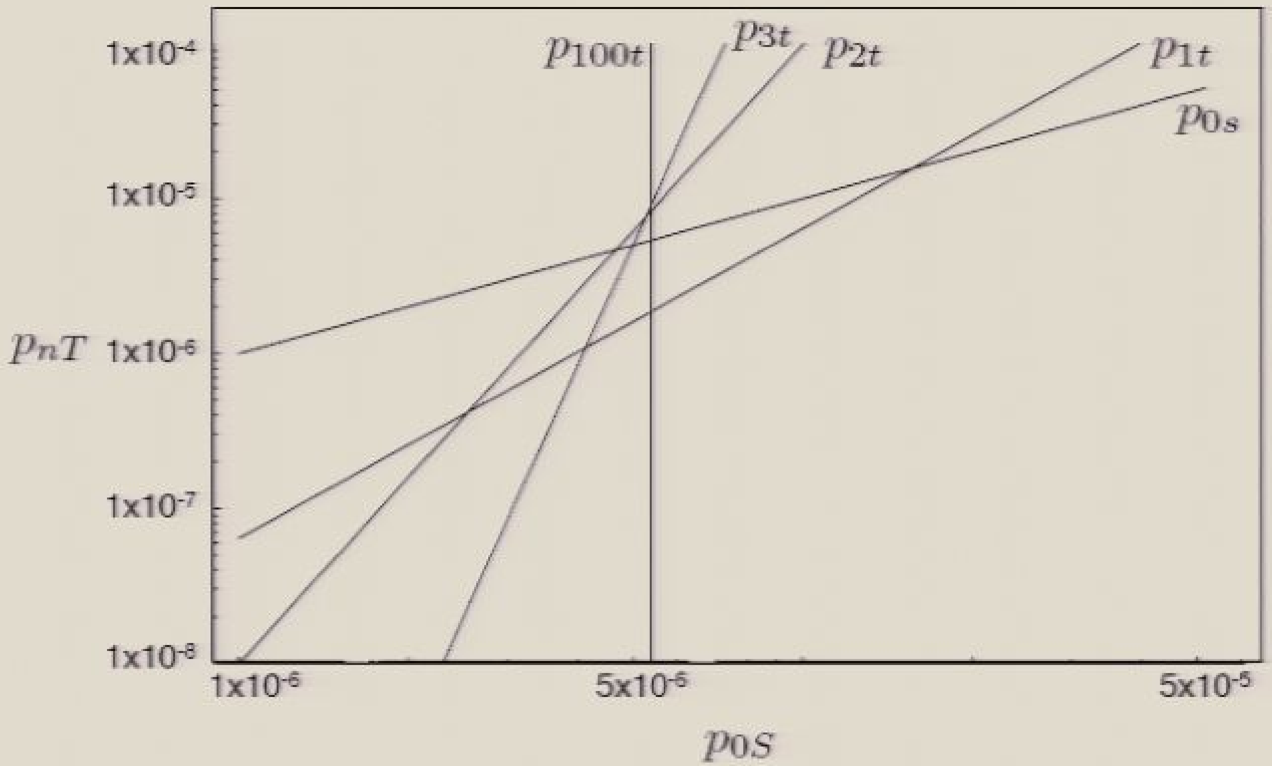

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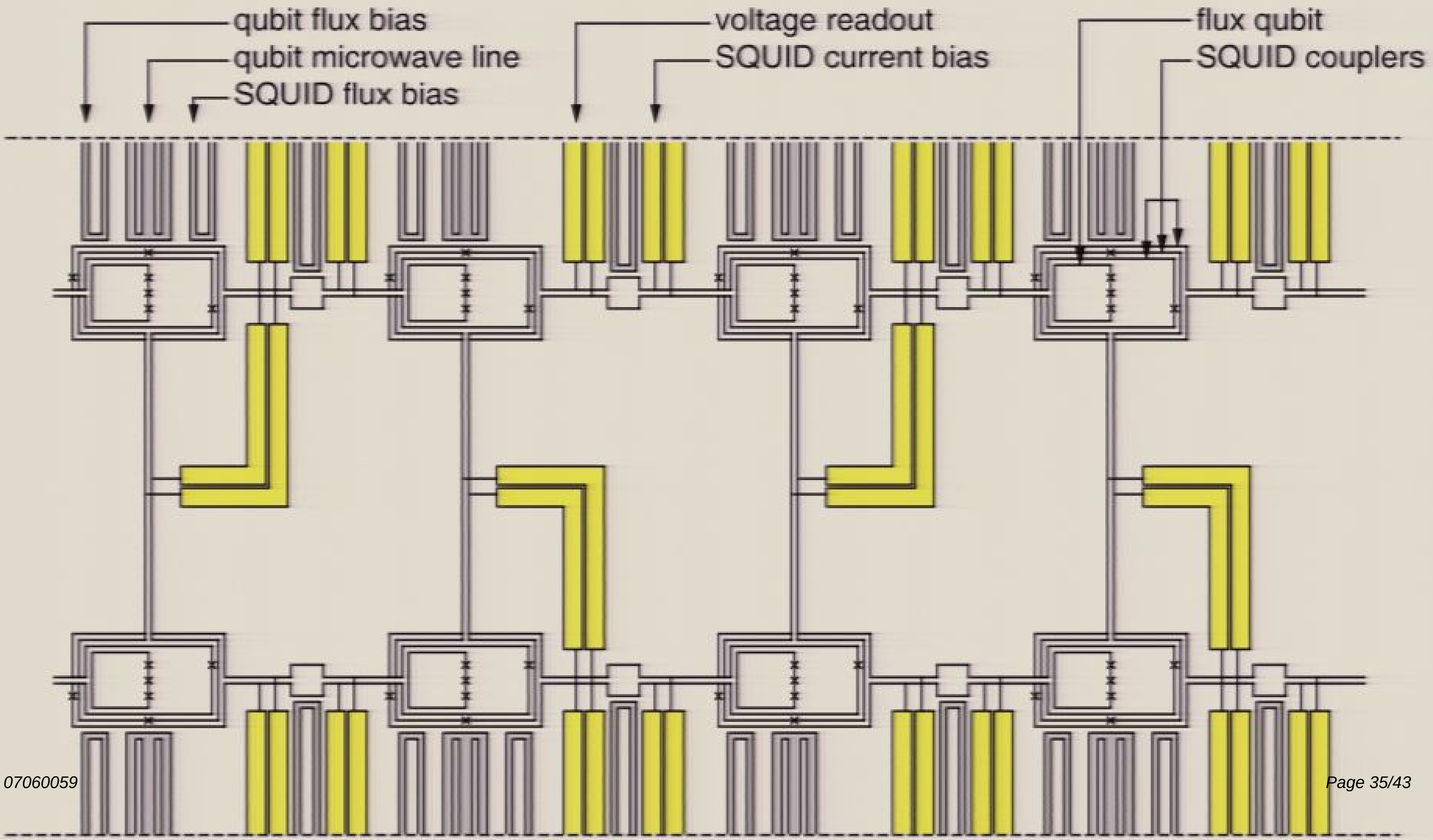
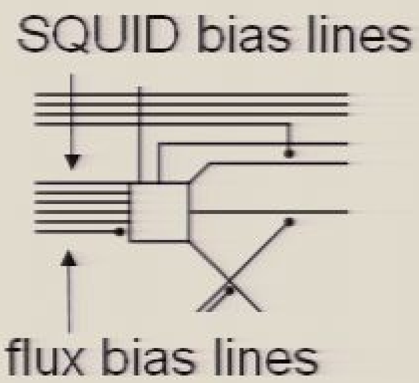
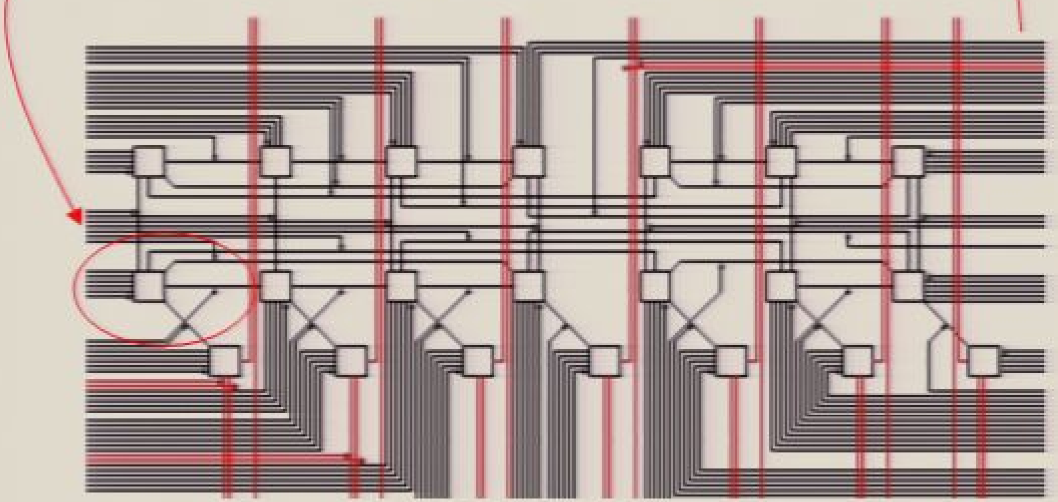
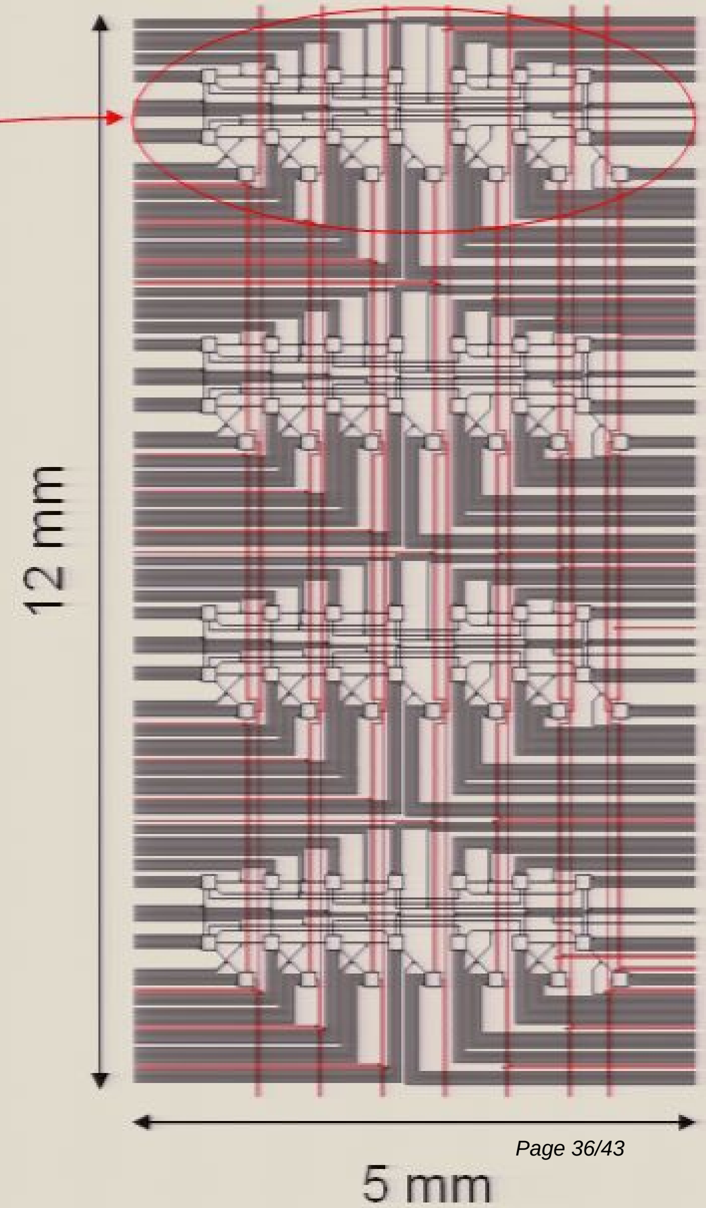


Level 2 circuitry

- Must control each qubit



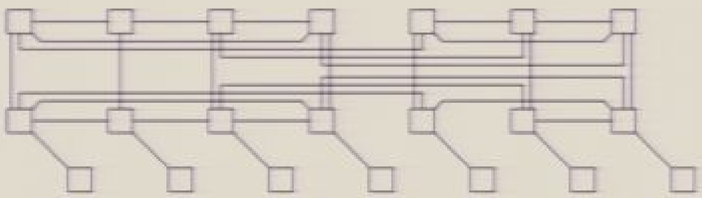




- 1 wire per 40 μm
- Fowler et al., cond-mat/0702620

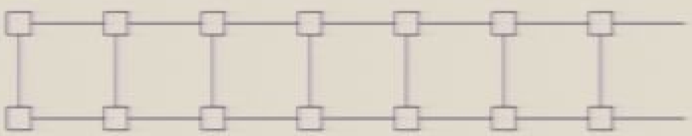
Three universal gate sets

- Non-local network



	$i=m$	$i=S$	$i=r$	depth
$j=m$	$206+28t_r$	100	28	$15+2t_r$
$j=S$	$398+56t_r$	207	56	$15+2t_r$
$j=T$	$1067+133t_r$	289	98	$75+10t_r$
$j=r$	$366+42t_r$	125	42	$30+4t_r$

- Bilinear network



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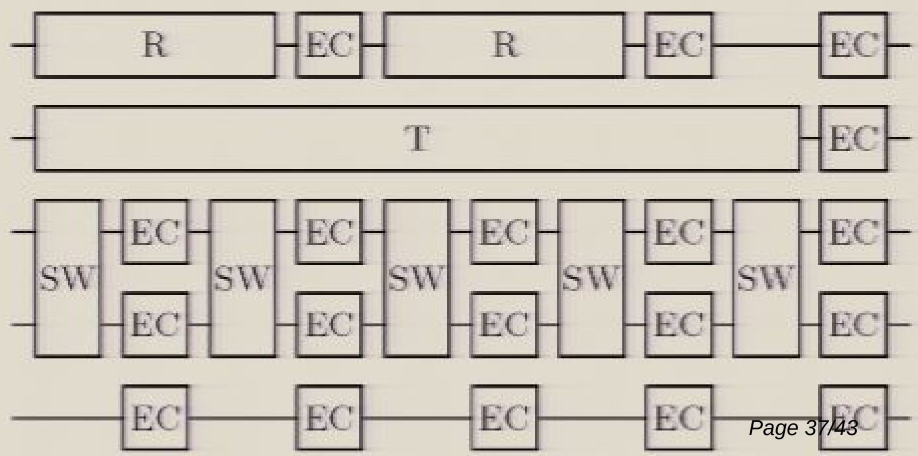

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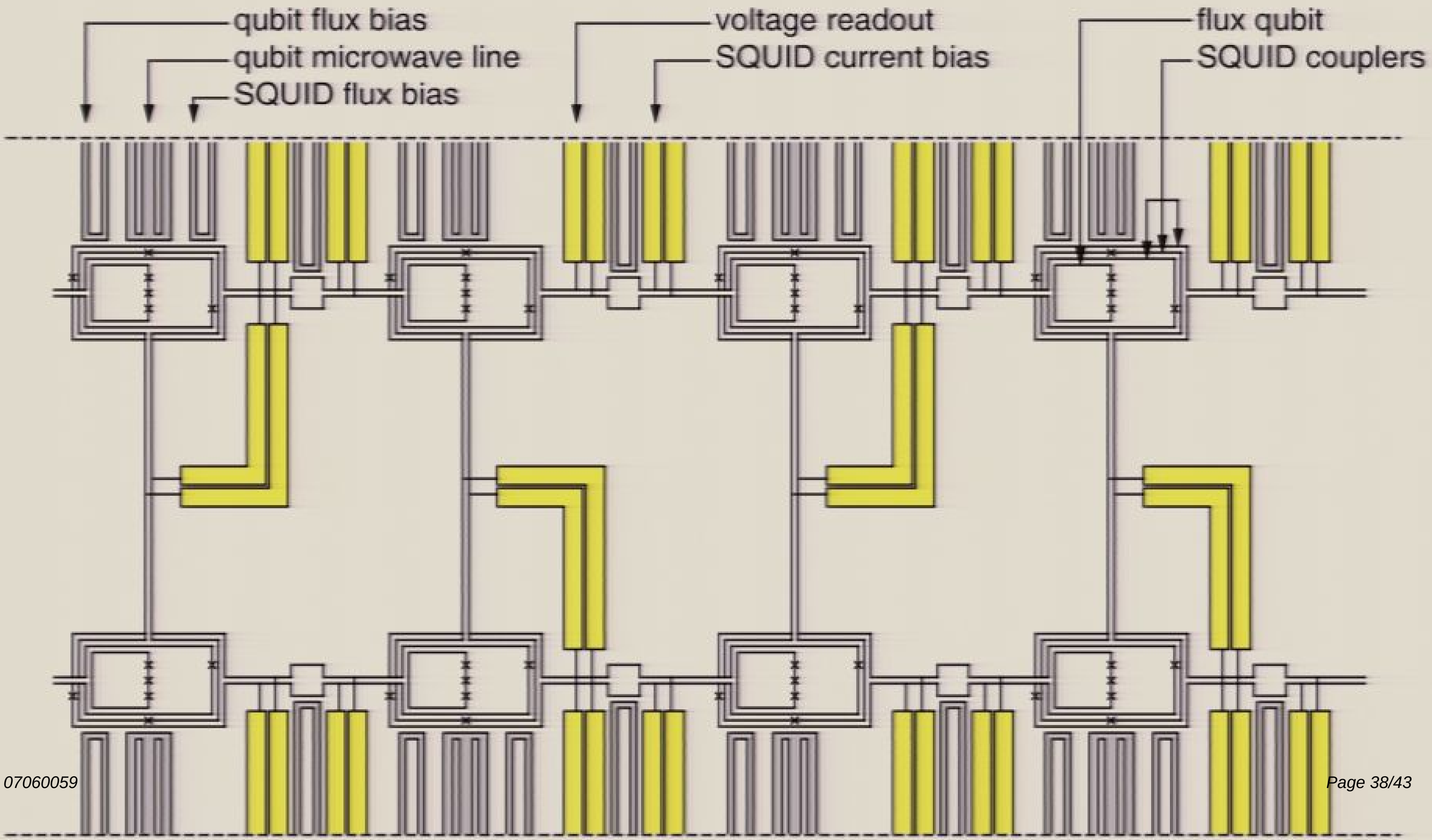
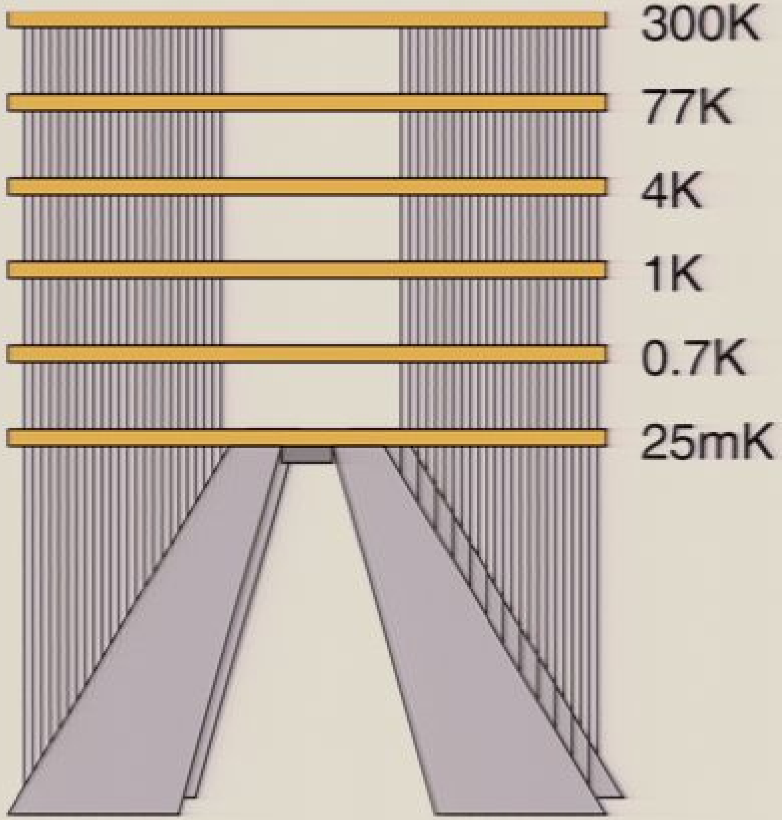


Further work



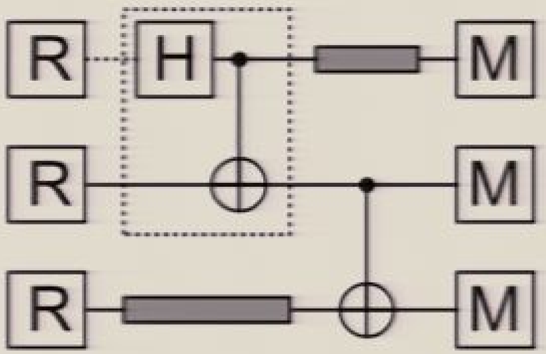
- Cooling – details
- Wire density – serious limitation
- Crosstalk and shielding
- Interchip spanning schemes
- Algorithms without error correction

Conclusion

- There is no universal threshold of 10^{-4}
- Without long-range interactions, threshold much lower
- For flux qubit architecture, threshold ~ 5×10^{-6}
- Implies gate error rates of ~ 10^{-7} needed
- May need to compute without error correction

Calculating thresholds

- Random example pretending to cope with one error



- Resets: 3
- Gates: 2
- Waits: 2
- Measurements: 3

$$
\begin{aligned}
p_{fail} &= 1 - p_{success} \\
&= 1 - (1 - p_{reset})^3 (1 - p_{gate})^2 (1 - p_{wait})^2 (1 - p_{meas})^3 \\
&\quad - p_{reset} (1 - p_{reset})^2 (1 - p_{gate})^2 (1 - p_{wait})^2 (1 - p_{meas})^3 \\
&\quad - p_{gate} (1 - p_{reset})^3 (1 - p_{gate}) (1 - p_{wait})^2 (1 - p_{meas})^3 \\
&\quad - p_{wait} (1 - p_{reset})^3 (1 - p_{gate})^2 (1 - p_{wait}) (1 - p_{meas})^3 \\
&\quad - p_{meas} (1 - p_{reset})^3 (1 - p_{gate})^2 (1 - p_{wait})^2 (1 - p_{meas})^2
\end{aligned}
$$

Bilinear details

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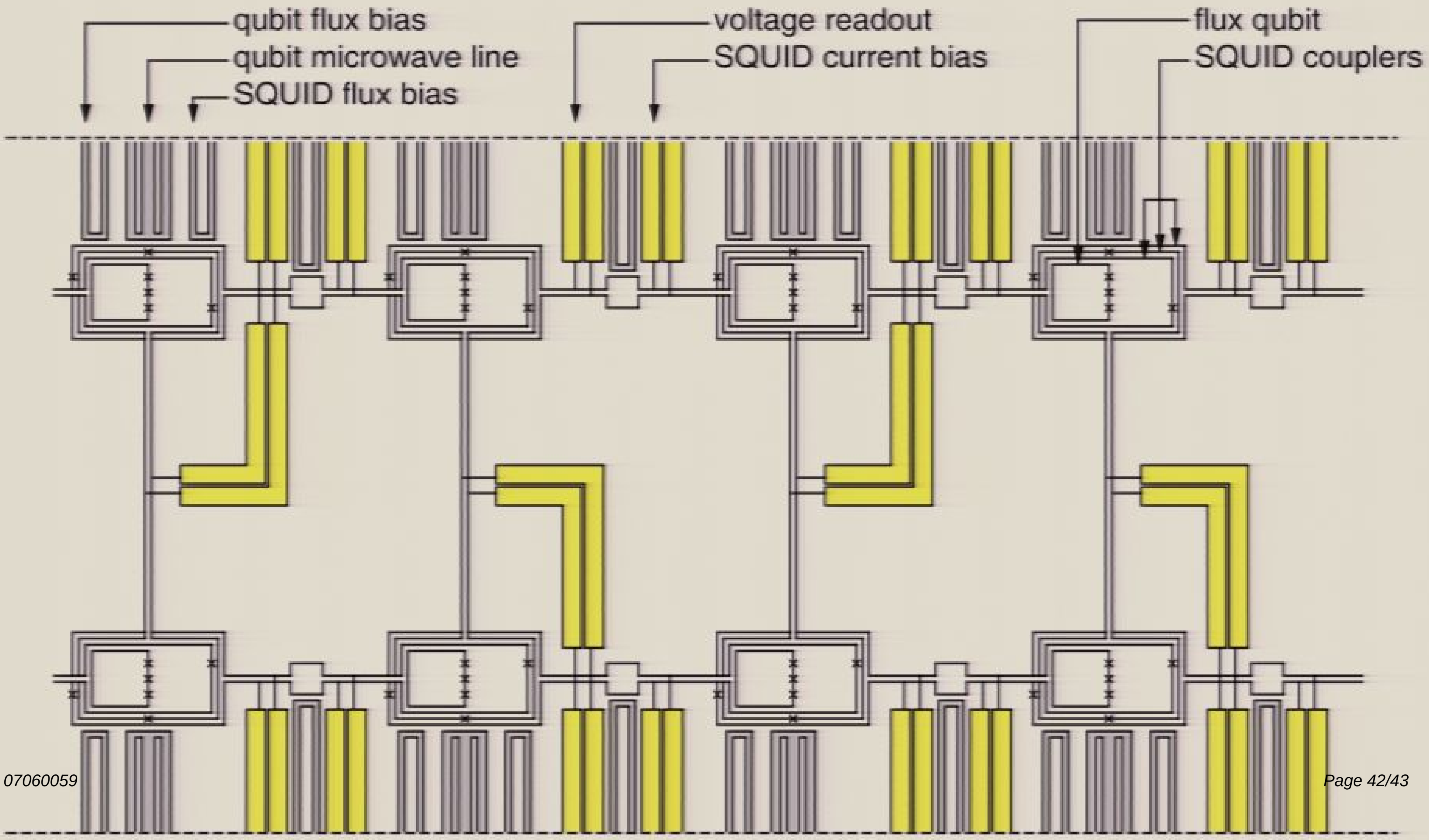

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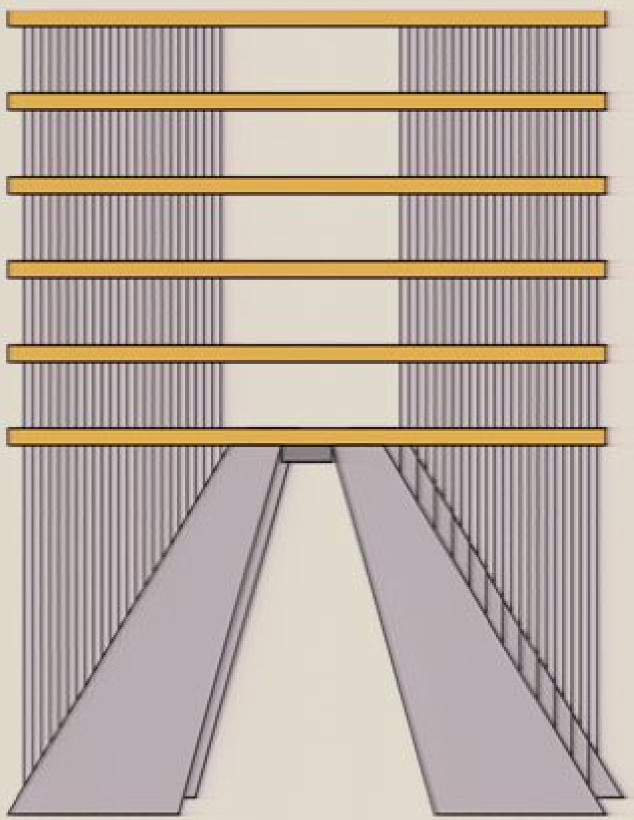

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