

Title: Quantum Error Correction 8B

Date: Feb 27, 2007 05:00 PM

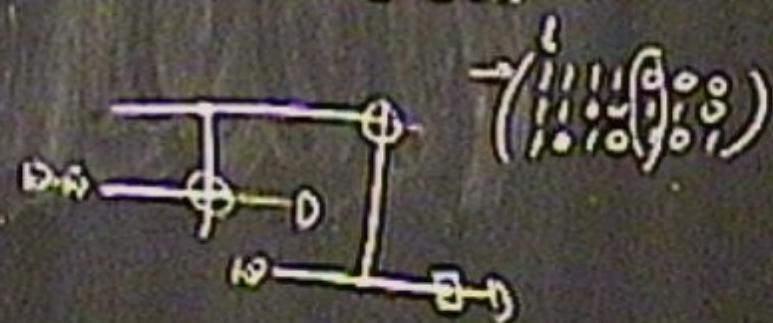
URL: <http://pirsa.org/07020029>

Abstract: Equivalence of fault-tolerant circuit to less noisy unencoded circuits, threshold theorem, calculation of the threshold.



Corollary: For a truncated exRec, good \Rightarrow correct.

Proof: Insert EC steps w/ no errors to replace truncated ones.





Assume all exRecs
are good.

Thm. [Good \Rightarrow Correct]: For a good exec.

Digitized by srujanika@gmail.com

$\neg [E \rightarrow D] \vdash \neg [E] \rightarrow D$

- "Correctness"

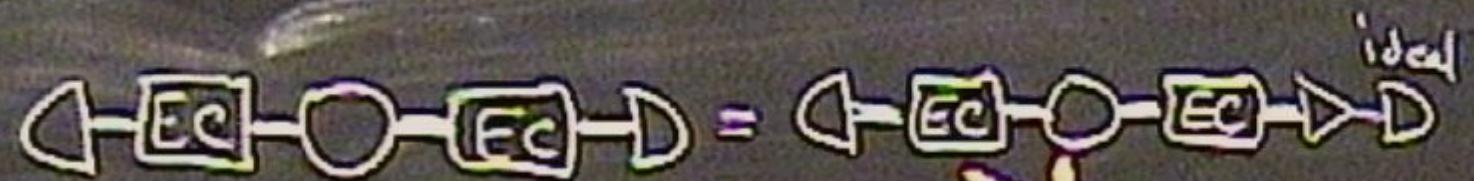
Proof

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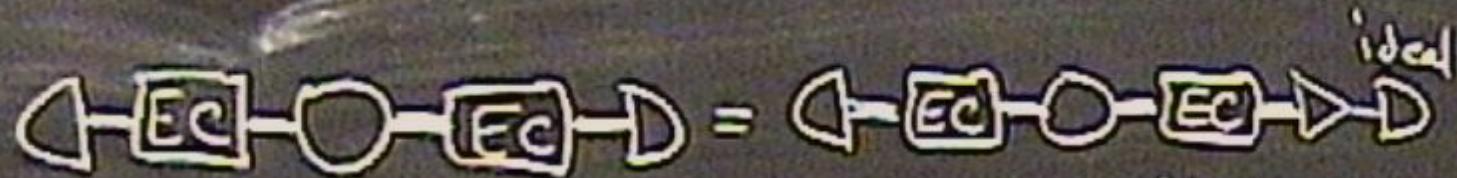
ج

(gate 1) - କୁର୍ମାନ୍ତିରାଜୁ - (gate 2) - କୁର୍ମାନ୍ତିରାଜୁ -



Assume all exRecs
are good.





Assume all exRecs
are good.

$$\leftarrow \boxed{Ec} - \circ - \boxed{Ec} \rightarrow D = \leftarrow \boxed{Ec} - \circ - \boxed{Ec} \rightarrow^{\text{ideal}} D$$

Assume all exRecs
are good.

$$= \leftarrow \boxed{Ec} \rightarrow^{\text{ideal}} D - \circ \rightarrow D = \leftarrow \overset{\text{ideal}}{O} \rightarrow D$$

$$\langle \boxed{E} \rangle - O - \boxed{E} \rightarrow D = \langle \boxed{E} \rangle - O - \boxed{E} \rightarrow^{\text{ideal}} D$$

Assume all exRecs are good.

$$= \langle \boxed{E} \rangle - D - O \rightarrow^{\text{ideal}} D = \langle O \rangle - D$$

Bad exRecs: wk

$$\neg \text{[Ec]} - \text{O} - \text{[Ec]} \rightarrow D = \neg \text{[Ec]} - \text{O} - \text{[Ec]} \xrightarrow{\text{ideal}} D$$

Assume all execs
are good.

$$= \neg \text{[Ec]} \xrightarrow{\text{ideal}} D - \text{O} \rightarrow D = \neg \text{O} \rightarrow D$$

Bad execs: We would like to move ideal decoder
through bad exec to get faulty gate:

$$\neg \text{[Ec]} - \text{O} - \text{[Ec]} \rightarrow D = \neg \text{O} \rightarrow D - \star$$

$$\leftarrow \boxed{Ec} - O - \boxed{Ec} \rightarrow D = \leftarrow \boxed{Ec} - O - \boxed{Ec} \xrightarrow{\text{ideal}} D$$

Assume all exRecs
are good.

Bad exRecs: We would like to move ideal decod
through bad exRec to get faulty gate:

$$-\boxed{Ec} - O - \boxed{Ec} \rightarrow = -\boxed{O} \rightarrow \times$$

But, error in decoded gate depends

$$\leftarrow \boxed{Ec} - \bigcirc - \boxed{Ec} \rightarrow D = \leftarrow \boxed{Ec} - \bigcirc - \boxed{Ec} \rightarrow \overset{\text{ideal}}{D}$$

Assume all exRecs
are good.

$$\rightarrow = \leftarrow \boxed{Ec} \rightarrow \overset{\text{ideal}}{D} - \bigcirc - \overset{\text{ideal}}{D} = \leftarrow \overset{\text{ideal}}{O} - \overset{\text{ideal}}{D}$$

Bad exRecs: We would like to move ideal decoder
through bad exRec to get faulty gate:

$$\rightarrow \boxed{Ec} - \bigcirc - \boxed{Ec} \rightarrow D = \rightarrow \boxed{Ec} \rightarrow \bigcirc \rightarrow$$

But, error in decoded gate depends on syndrome of incoming data
E.g. For 7-qubit code, there is 1 bit flip error & 1 phase error in exRec.

$$\langle \text{Ec} \rangle \circ \text{O} \circ \langle \text{Ec} \rangle \rightarrow D = \langle \text{Ec} \rangle \circ \text{O} \circ \langle \text{Ec} \rangle \xrightarrow{\text{ideal}} D$$

Assume all exRecs are good.

$$= \langle \text{Ec} \rangle \rightarrow \text{O} \rightarrow D = \langle \text{O} \rightarrow D \rangle^{\text{ideal}}$$

Bad exRecs: We would like to move ideal decoder through bad exRec to get faulty gate:

$$\neg \langle \text{Ec} \rangle \circ \text{O} \circ \langle \text{Ec} \rangle \rightarrow D = \neg \langle \text{Ec} \rangle \rightarrow \text{O} \rightarrow D$$

But, error in decoded gate depends on syndrome of incoming state.
 E.g.: For 7-qubit code, there is 1 bit flip error & 1 phase error in exRec.
 If incoming syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
 If incoming syndrome is a phase error, gate has phase error

E.g.: For 7-qubit code, there is 1 bit flip error & 1 phase error in case
If incoming syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
phase

Solution:

E.g.: For 7-qubit code, there is 1 bit flip error & 1 phase error in error.
If inverting syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
phase

Solution: Introduce *-decoder, which keeps syndrome

$$\overline{D} \xrightarrow{\text{(syndrome)}} \overline{D} = \overline{D}$$

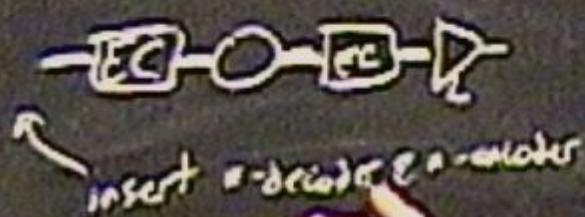
*-decoder w/ discarded syndrome
= ideal decoder.

E.g. For 7-qubit code, there is 1 bit flip error & 1 phase error in each
If incoding syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
phase

Solution: Introduce *-decoder, which keeps syndrome

$$\overline{D} \xrightarrow{\text{(syndrome)}} \overline{D}$$

*-decoder w/ discarded syndrome
= usual decoder.



E.g. For 7-qubit code, there is 1 bit flip error & 1 phase error in circuit.
 If inverting syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
 phase

Solution: Introduce *-decoder, which keeps syndrome

$$\neg \sum_{\text{(syndrome)}} = \neg \sum_{\oplus}$$

*-decoder w/ discarded syndrome
 = ideal decoder.

$$\neg EC \rightarrow \neg \sum_{\oplus} = \neg \sum_{\oplus} \otimes \neg$$

insert *-decoder & -inverter

E.g.: For 7-pubit code, there is 1 bit flip error & 1 phase error or vice versa.
 If inoring syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
 phase

Solution: Introduce π -decoder, which keeps syndrome

$$\neg \sum_{i=1}^7 (\text{syndrome}) = \neg \sum_{i=1}^7 \neg D_i = \neg D$$

π -decoder w/ discarded syndrome
 → ideal decoder.

$$\neg EC \circ \neg \sum_{i=1}^7 \neg D_i = \neg \sum_{i=1}^7 \neg D_i \oplus \neg D \quad (\text{For bad corrections})$$

insert π -decoder & π -encoder

Correctness for ideal decoder \Rightarrow correctness for π -decoder

E.g. For 7-pubit code, there is 1 bit flip error & 1 phase error in case
 If incoming syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
 phase

Solution: Introduce π -decoder, which keeps syndrome

$$-\sum \text{(syndrome)} = \overline{\sum} = \overline{D}$$

π -decoder w/ discarded syndrome
 = ideal decoder.

$$-EC \circ EC \circ D = -\overline{D} \oplus \overline{S} \quad (\text{For bad cases})$$

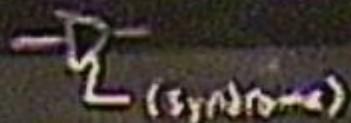
insert π -decoder & π -encoder

Correctness for ideal decoder \Rightarrow correctness for π -decoder

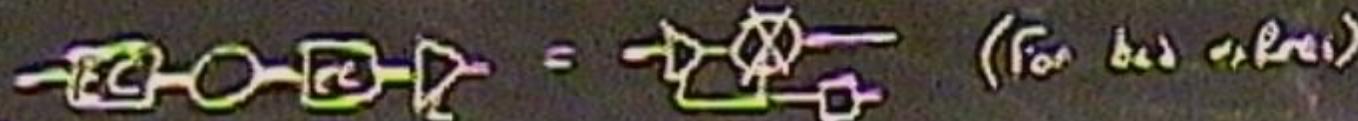
$$-EC \circ EC \circ D = -\overline{D} \circ \overline{S} \quad \text{for all } S \Rightarrow \text{syndrome not corr.}$$

* output

E.g. For 7-pubit code, there is 1 bit flip error & 1 phase error in each
If memory syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
phase



*-decoder w/ discarded syndrome
→ ideal decoder



Correctness for ideal decoder \Rightarrow correctness for \neg -decoder



\neg decoder not corrected with the
(unless already corrected for input)

E.g.: For 7-pubit code, there is 1 bit flip over 8 phase error in case
 If incoming syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
 phase

— (syndrome)

* decoder w/ discarded syndrome

= ideal decoder

$$-\text{EC} \circ -\text{EC} \circ -\text{D} = -\text{D} \oplus \text{O} \quad (\text{For bad cases})$$

insert = decode & -inverter

Correctness for ideal decoder \Rightarrow correctness for π -decoder

$$-\text{EC} \circ -\text{O} \circ -\text{EC} \circ -\text{D} = -\text{EC} \circ -\text{D} \quad \text{for all input states}$$

⇒ syndrome not corrected
 (unless already corrected) for π

$$\Rightarrow -\text{EC} \circ -\text{O} \circ -\text{EC} \circ -\text{D} = -\text{EC} \circ -\text{D}$$

It memory syndrome, no error, "correct" or "incorrect" phase errors

Solution: Introduce *-decoder, which keeps syndrome

$$-\sum_{i=1}^n D_i = -D$$

(syndrome)

$$-\sum_{i=1}^n D_i = -D$$

*-decoder w/ disordered syndrome
= ideal decoder

$$-EC \circ O \square EC \rightarrow D = -D \otimes \square \quad (\text{For bad entries})$$

insert *-decoder & *-encoder

Correctness for ideal decoder \Rightarrow correctness for *-decoder

$$-EC \circ O \square EC \rightarrow D = -D \xrightarrow{\text{ideal}} D \quad \text{for all input states}$$

\Rightarrow syndrome not correlated with
(unless already correlated for input)

$$\Rightarrow -ED \circ O \square EC \rightarrow D = -EC \rightarrow D$$

It memory syndrome, to error, it corrects it phase 100% a phase error

Solution Introduce π -decoder, which keeps syndrome

$$-\overline{D}$$

(syndrome)

$$\overline{\overline{D}} = -\overline{D}$$

π -decoder w/ discarded syndrome
= ideal decoder.

$$-\overline{EC} \circ \overline{D} = -\overline{D} \otimes \overline{O} \quad (\text{For bad cRcs})$$

insert π -decoder & π -encoder

Correctness for ideal decoder \Rightarrow correctness for π -decoder

$$-\overline{EC} \circ \overline{O} \circ \overline{EC} \circ \overline{D} = -\overline{EC} \circ \overline{D} \quad \text{for all input states}$$

\Rightarrow syndrome not correlated with the output
(unless already correlated for input)

$$\Rightarrow -\overline{ED} \circ \overline{O} \circ \overline{EC} \circ \overline{D} = -\overline{EC} \circ \overline{D} \quad (\text{similar for truncated cRcs})$$

It is very difficult, if not impossible, to estimate the precise error

Solution: Introduce *-decoder, which keeps syndrome

$$\xrightarrow{\text{D}} \text{(syn)rome} \quad \xrightarrow{\text{D}} = \xrightarrow{\text{D}} \begin{array}{l} \text{*-decoder w/ discarded syndrome} \\ \text{* ideal decoder.} \end{array}$$

$-E\text{O}-\text{O}-E-\text{D} = -\text{D}-\text{O}-E$ (For bed express)

insert = dropper - snaker

Correctness for ideal decoder \Rightarrow correctness for π -decoder

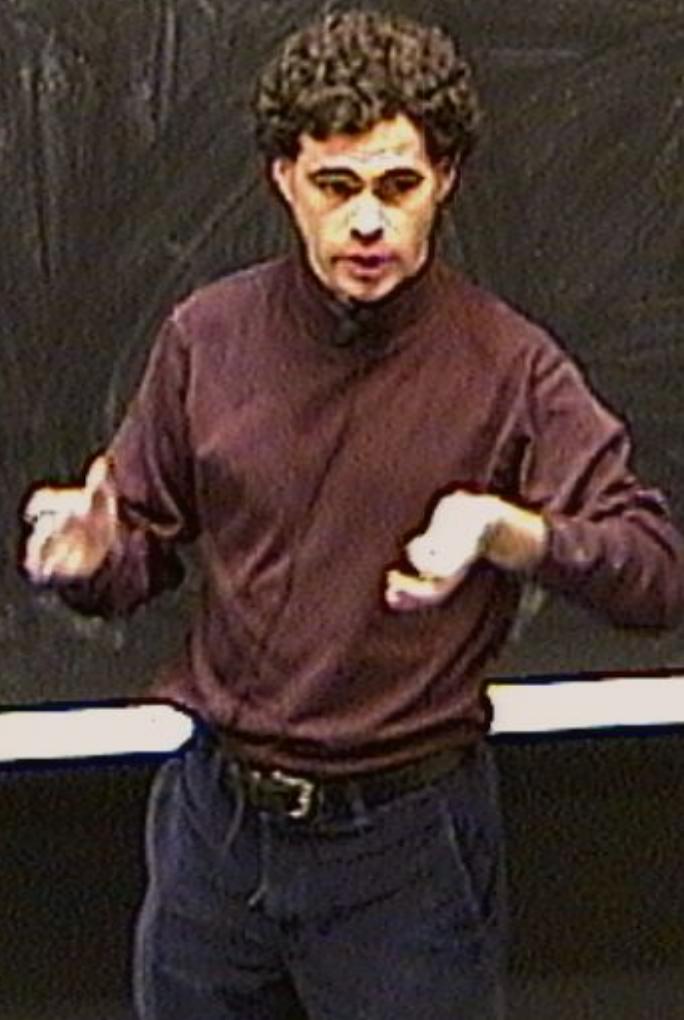
$$\text{nos for ideal decoder} \Rightarrow \text{correctness} \\ -E_0 - O - E_1 = -E_0 \Rightarrow \text{for all input states} \\ \Rightarrow \text{s syndrom not corrected at} \\ \text{input variable for input}$$

- for all input states
- \Rightarrow syndrome not correlated with the output
(unless already corrected for input)

$$\Rightarrow -\boxed{EC} \text{-O-} \boxed{EC} \text{-D} = -\boxed{EC} \text{-D} \xrightarrow{\text{O}} \quad (\text{similar for truncated cRns})$$

(unless already corrected for input
(similar for truncated errors)

What is the probability of a bad $\text{exRec} \rightarrow$
Need $t+1$ bad locations



What is the Probability of a bad exRec?

Need $t+1$ bad locations, P^{t+1} of having errors in a particular set

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There are $\binom{A}{t+1}$ sets, where $A = \#$ locations in exRec

$$P(\text{Bad}) \leftarrow \binom{A}{t+1} P^{t+1}$$

What is the Probability of a bad exRec?

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What is the Probability of a bad exec?

Need $t+1$ bad locations, P^{t+1} of having errors in a particular set

There are $\binom{A}{t+1}$ sets, where $A = \#$ locations in exec

$$P(\text{Bad}) \leq \binom{A}{t+1} P^{t+1}$$

E.g.: CNOT exec for 7-qubit a

What is the probability of a bad error?

Need $T+1$ bad locations, P^{T+1} of having errors in a particular set.

There are $\binom{A}{T+1}$ sets, where $A = \#$ locations in error

$$P(\text{Bad}) \leq \binom{A}{T+1} p^{T+1}$$

E.g.: CNOT error for 7-qubit code, $T=1$



\rightarrow 7 CNOT gates, 4 EC

$$A =$$

$$P(\text{Bad}) \leq \binom{A}{2} p^2$$



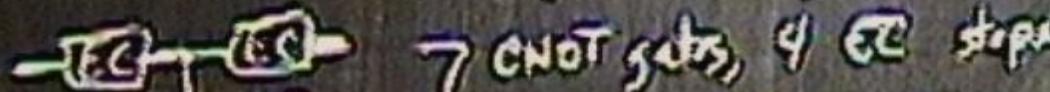
What is the Probability of

Need $t+1$ bad locations, P of having errors in a particular set

There are $\binom{A}{t+1}$ sets, where $A=H$ locations in error

$$P(\text{Bad}) \leq \binom{A}{t+1} p^{t+1}$$

E.g.: CNOT exRee for 7-qubit code, $t=1$ $P(\text{Bad}) \leq \binom{7}{2} p^2$



7 CNOT gates, 4 EC steps

A quantum circuit diagram with three horizontal lines representing qubits. The top line has a green square at its left end. The middle line has a green square at its right end. The bottom line has a green square at its left end. Two CNOT gates are placed between the first and second qubits. The first CNOT gate has its control on the top line and target on the middle line. The second CNOT gate has its control on the middle line and target on the bottom line.

$A=7$, $B=4$, $B=$ # locations in EC

Sometimes we are interested in exRees which are missing some or more trailing EC steps. These

15> 15> 15>



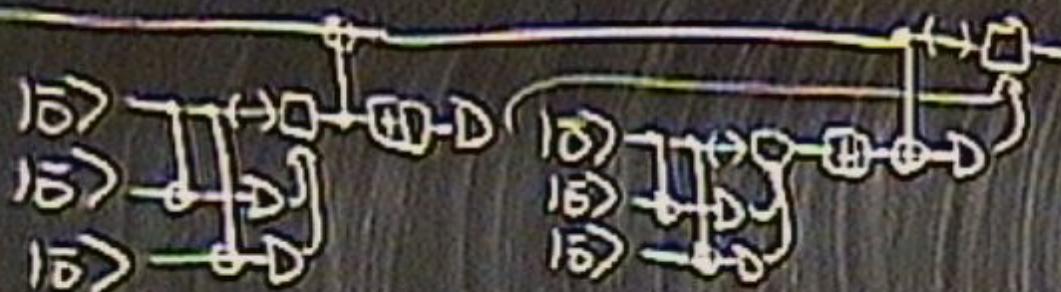
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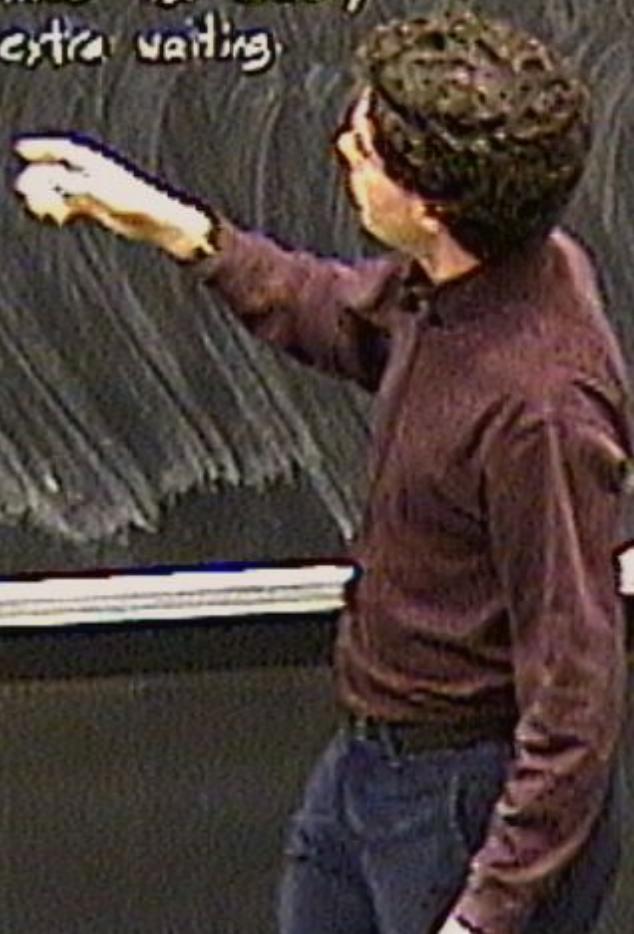
15> $\overline{1} \overline{2} \overline{3} \overline{4}$
15> $\overline{1} \overline{2} \overline{3}$
15> $\overline{1} \overline{2}$

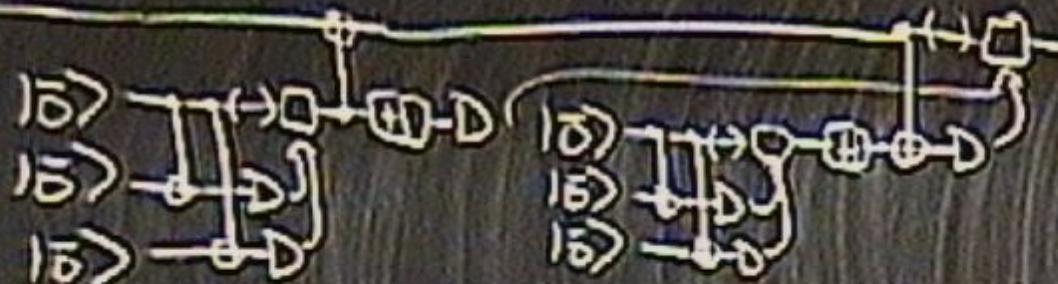
15> $\overline{1} \overline{2}$
15> $\overline{1}$





Note: Prepare ancillas for exactly when
needed to avoid extra waiting.

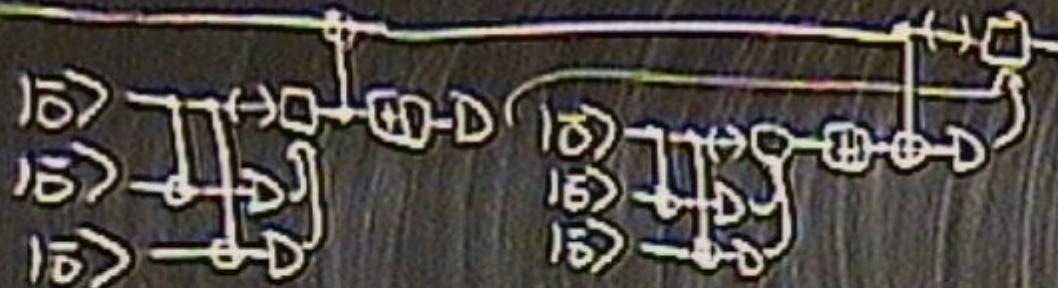




$$6 \times 7 = 42 \text{ CNOTs}$$

Note: Prepare ancillas for exactly when needed to avoid extra waiting.





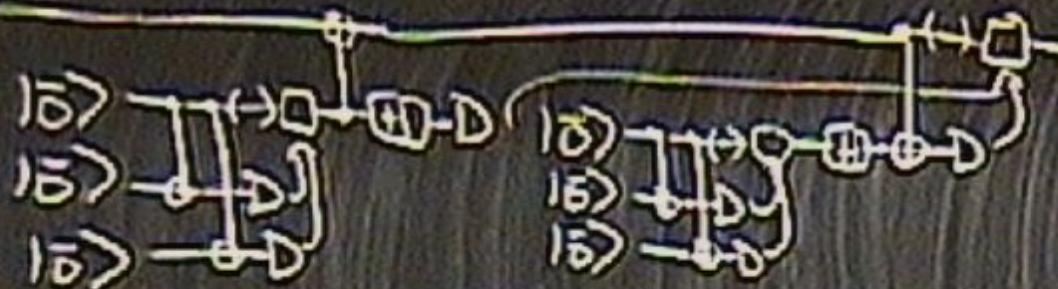
Note: Prepare ancillas for exactly when needed to avoid extra waiting.

$$6 \times 7 = 42 \text{ CNOTs}$$

$$5 \times 7 = 35 \text{ single-qubit gates}$$

$$3 \times 7 = 21 \text{ waits}$$

$$6 \times 7 = 42 \text{ measurements}$$



Note: Prepare ancillas for exactly when needed to avoid extra waiting.

$$6 \times 7 = 42 \text{ CNOTs}$$

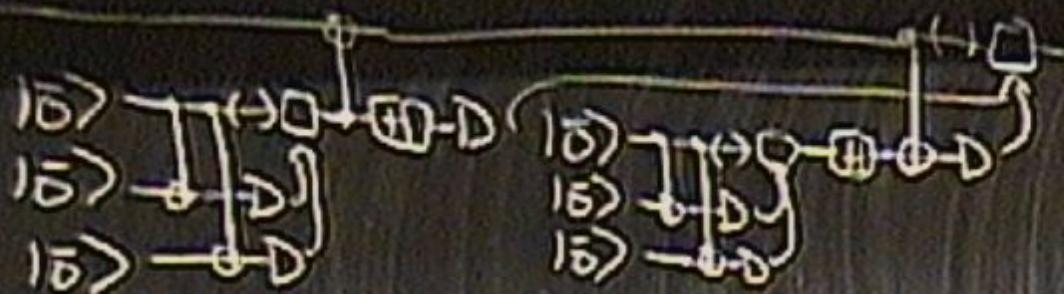
$$5 \times 7 = 35 \text{ single-qubit gates}$$

$$3 \times 7 = 21 \text{ waits}$$

$$6 \times 7 = 42 \text{ measurements}$$

$$6 \text{ preparations}$$

$B =$



Note: Prepare ancillas for exactly when
needed to avoid extra waiting.

$|{\bar{0}}\rangle$ encoder (non-FT):

$$6 \times 7 = 42 \text{ CNOTs}$$

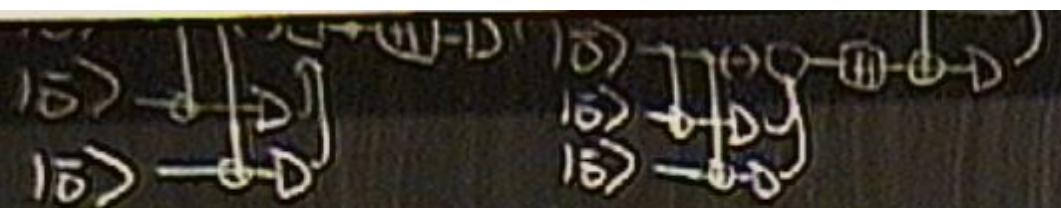
$$5 \times 7 = 35 \text{ single-qubit gates}$$

$$3 \times 7 = 21 \text{ waits}$$

$$6 \times 7 = 42 \text{ measurements}$$

$$6 \text{ preparations}$$

$$B = 140 + 6C, \quad C = \# \text{ locations in } |{\bar{0}}\rangle \text{ prep}$$



Note: Prepare ancillas for exactly when needed to avoid extra waiting.

$5 \times 7 = 35$ single-qubit gates

$3 \times 7 = 21$ waits

$6 \times 7 = 42$ measurements

6 preparations

$B = 140 - 6C$, $C = \# \text{ locations in } |\bar{0}\rangle \text{ prep}$

$|\bar{0}\rangle$ encoder (non-FT):

$|\bar{0}\rangle -$

$|\bar{0}\rangle -$

$|\bar{0}\rangle -$

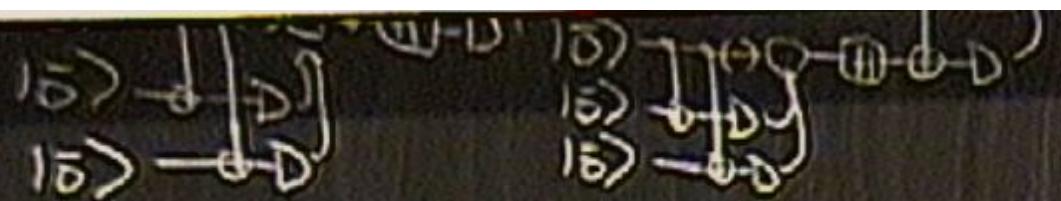
$|\bar{1}\rangle - \bar{\text{II}}$

$|\bar{1}\rangle -$

$|\bar{1}\rangle - \bar{\text{II}}$

$|\bar{1}\rangle - \bar{\text{II}}$





Note: Prepare ancillas for exactly when needed to avoid extra waiting.

$$5 \times 7 = 35 \text{ single-qubit gates}$$

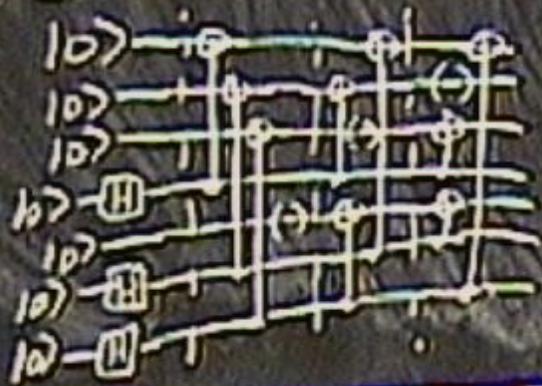
$$3 \times 7 = 21 \text{ waits}$$

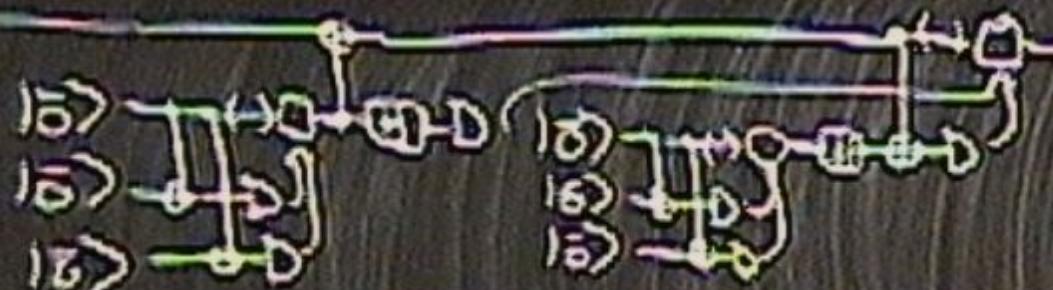
$$6 \times 7 = 42 \text{ measurements}$$

$$6 \text{ preparations}$$

$$B = 140 - 6C, \quad C = \# \text{ locations in } |00\rangle \text{ prep.}$$

$|00\rangle$ encoder (non-FT):





Note: Prepare ancillas for exactly when needed to avoid extra waiting.

$$4 \cdot 7 = 42 \text{ CNOTs}$$

$$5 \cdot 7 = 35 \text{ single bit gates}$$

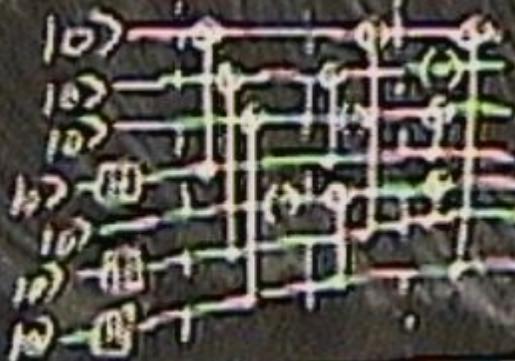
$$3 \cdot 7 = 21$$

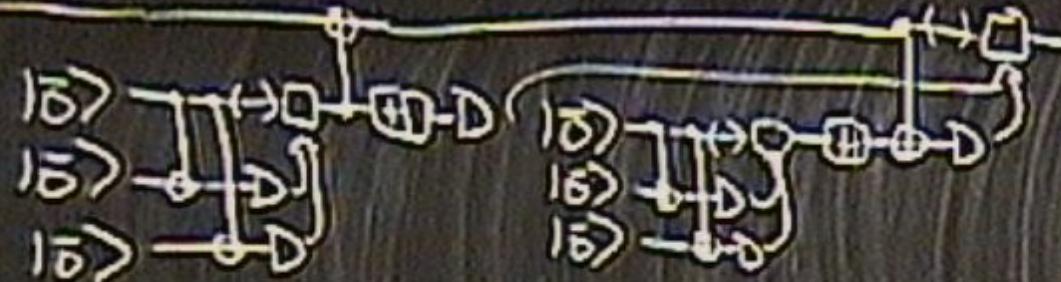
$$7 \cdot 7 = 49$$

$$6 \text{ prep gates}$$

$$B = 140 - 6C, \text{ where } C \text{ is the number of controls in}$$

15) encoder (non-FT):





Note: Prepare ancillas for exactly when needed to avoid extra waiting.

$$6 \times 7 = 42 \text{ CNOTs}$$

$$5 \times 7 = 35 \text{ single-qubit gates}$$

$$3 \times 7 = 21 \text{ waits}$$

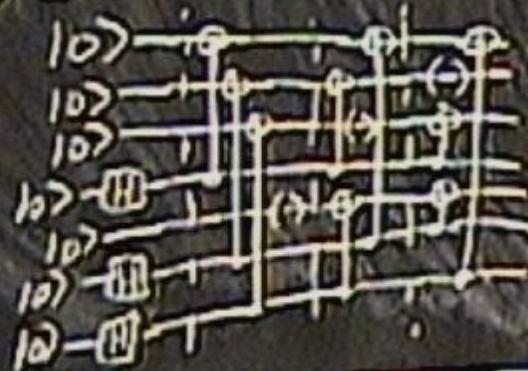
$$6 \times 7 = 42 \text{ measurement}$$

$$6 \text{ preparations}$$

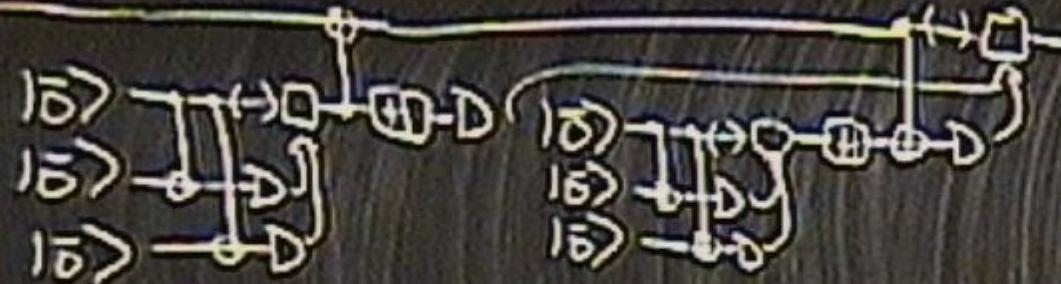
$$B = 140 + 6C, C = 7$$

$|0\rangle$

$|0\rangle$ encoder (non-FT):



9 CNOTs
3 single-qubit gates
3 waits
7 $|0\rangle$ prep



Note: Prepare ancillas for exactly when needed to avoid extra waiting.

$$6 \times 7 = 42 \text{ CNOTs}$$

$$5 \times 7 = 35 \text{ single-qubit gates}$$

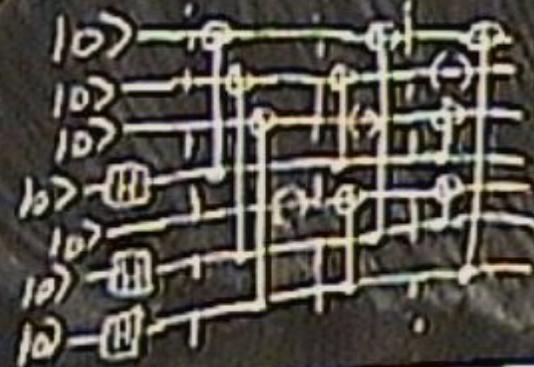
$$3 \times 7 = 21 \text{ waits}$$

$$6 \times 7 = 42 \text{ measurements}$$

$$6 \text{ preparations}$$

$$B = 140 + 6C, C = \frac{\text{number of qubits}}{10}$$

$|10\rangle$ encoder (non-FT):



9 CNOTs
3 single-qubit gates
2 waits
7 $|10\rangle$ prep

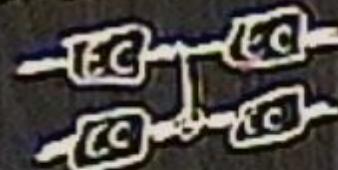
What is the Probability of a bad exRec?

Need $T+1$ bad locations, P^{T+1} of having errors in a particular set.

There are $\binom{A}{T+1}$ sets, where $A = \#$ locations in exRec

$$P(\text{Bad}) \leq \binom{A}{T+1} p^{T+1}$$

E.g.: CNOT exRec for 7-qubit code, $T=1$ $P(\text{Bad}) \leq \binom{A}{2} p^2$



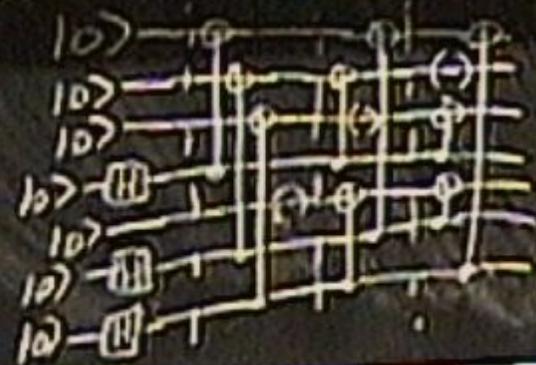
7 CNOT gates, 4 EC steps

$$A = 7 - 4B, \quad B = \# \text{ locations in EC}$$

$P(\text{Bad}) \leq \binom{N}{2} P^2$
 E.g.: CNOT circuit for 7-qubit code, $T=1$

 $A = 7 - 4B, B = \# \text{locations in EC}$
 $= 1071$

15) encoder (non-FT):



9 CNOTs
 $3 \text{ single-qubit gates}$
 2 units
 $\Rightarrow \beta = 266$
 $C = 21$
 $\Rightarrow 107 \text{ qRIP}$

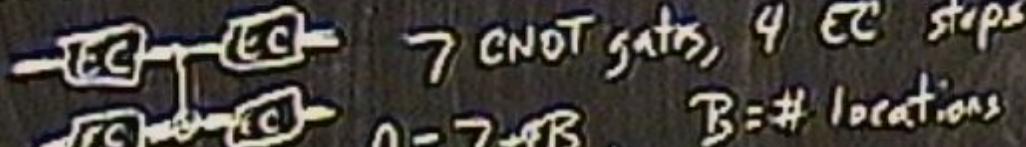
What is the Probability of a bad exec

Need $T+1$ bad locations, P^{T+1} of having errors in a particular set

There are $\binom{A}{T+1}$ sets, where $A = \#$ locations in exec

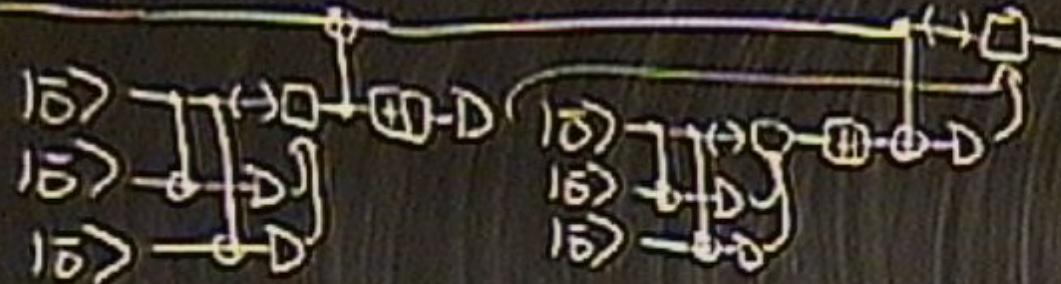
$$P(\text{Bad}) \leftarrow \binom{A}{T+1} P^{T+1}$$

E.g.: CNOT exec for 7-qubit code, $T=1$ $P(\text{Bad}) \leq \binom{A}{2} P^2 =$



$$\begin{aligned} A &= 7 - TB, & B &= \# \text{ locations in EC} \\ &= 1071 \end{aligned}$$

$$\begin{array}{c} 107 \\ - 104 \\ \hline 3 \end{array}$$



Note: Prepare ancillas for exactly when needed to avoid extra waiting.

$$6 \times 7 = 42 \text{ CNOTs}$$

$$5 \times 7 = 35 \text{ single-qubit gates}$$

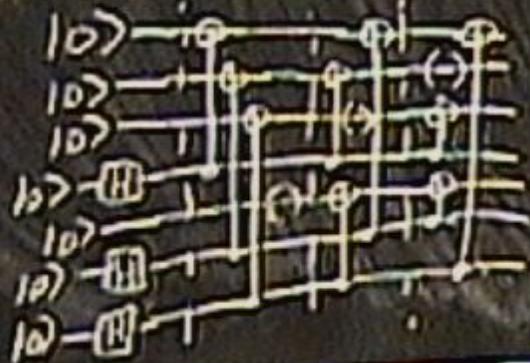
$$3 \times 7 = 21 \text{ waits}$$

$$6 \times 7 = 42 \text{ measurements}$$

6 preparations

$$\beta = 140 + 6C, \quad C = \# \text{locations in } |10\rangle \text{ prep}$$

$|10\rangle$ encoder (non-FT):



9 CNOTs
3 single-qubit gates
2 waits
7 |10> prep

$$C = 21$$

$$\Rightarrow \beta = 266$$

Prob. (multiple bad effects) - not independent



↳ Proto. (multiple bad effects) - not independent
 3 physical errors, but \geq 2 bad effects

Prob. (multiple bad errors) - not independent



3 physical errors, but \geq 2 bad errors

Truncation: Starting from end of FT circuit, truncated
any erRec that is followed by erRec. If the

Prob. (multiple bad errors) - not independent



3 physical errors, but ≥ 2 bad errors

Truncation: Starting from end of FT circuit, truncated
any erRec that is followed by a bad erRec. If the
truncated erRec is good, it counts as good for further truncations.

Prob. (multiple bad errors) - not independent



3 physical errors, but \geq bad errors

Truncation: Starting from end of FT circuit, truncated
any error that is followed by a bad error. If the
truncated error is good, it counts as good for further truncations.

E.g.: For 7-pubit code, there is 1 bit flip error & 1 phase error
 If incoming syndrome = 0, no error, if syndrome is a bit flip, gate has bit flip error
 phase error

Solution: Introduce *-decoder, which keeps syndrome

$$\neg D \xrightarrow{\text{(syndrome)}} \neg D = \neg D \quad \begin{matrix} \text{*-decoder} \\ \downarrow \text{discarded syndrome} \end{matrix}$$

→ ideal decoder

$$\neg EC \circ \neg D \circ \neg D \xrightarrow{\text{insert *-decoder & *-mutes}} \neg D \otimes \neg D \quad (\text{For bad cRcs})$$

Correctness for ideal decoder \Rightarrow correctness for *-decoder

$$\neg EC \circ \neg D \circ \neg EC \xrightarrow{\text{for all input states}} \neg D \circ \neg D \xrightarrow{\text{ideal}} \text{for all input states}$$

\Rightarrow syndrome not correlated with the output
 (unless already correlated for input)

$$\neg EC \circ \neg D \circ \neg EC \circ \neg D \xrightarrow{\text{similar for truncated cRcs}}$$



↳ Proto. (multiple bad effects) - not independent

~~FOB-GO~~

3 physical errors, but 2 bad effects

Truncation: Starting from end of FT circuit, truncated
Rec that is followed by a bad effect.
→ effect is good, it counts as good for further truncations.

Now if
This

Pr_{err} (multiple bad errors) - not independent



3 physical errors, but 2 bad erRecs

Truncation: Starting from end of FT circuit, truncated
any erRec that is followed by a bad erRec. If the
truncated erRec is good, it counts as good for further truncations.
Now prob (multiple bad errors) \leq \prod prob (each bad)

Thm (Lower reduction): A FT circuit can be replaced by a m
unenclosed circuit, with errors bounded by prob $p' \leq \left(\frac{1}{n} \vee p\right)^{t+1}$

(\curvearrowleft) Prob. (multiple bad errors) - not independent

~~GOOD~~

3 physical errors, but 2 bad errors

Truncation: Starting from end of FT circuit, truncated
any error that is followed by a bad error, If the
truncated error is good, it counts as good for further truncations.
Now prob. (multiple bad errors) \leq \prod prob (each bad)

Thm (Local reduction): A FT circuit can be replaced by a noisy
unreduced circuit, with errors bounded by prob $p' \leq (\frac{A}{nV})^{nV}$, where A is
the number of locations in the largest error.

Prob. (multiple bad errors) - not independent

~~BOB-OO~~

3 physical errors, but 2 bad errors

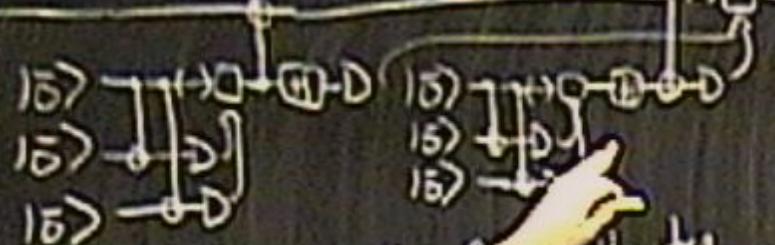
Truncation: Starting from end of FT circuit, truncated
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Thm (Local reduction): A FT circuit can be replaced by a noisy
uncluttered circuit, with errors bounded by prob $P' = \left(\frac{A}{nV}\right)^{t+1}$, where A is
the number of locations in the largest error.

syndrome

with the output

(CRs)



Note: Prepare ancillas if necessary
needed to avoid entangling



9 CNOTs
3 single-qubit gates
2 units
 $\frac{1}{2} 107 \text{ prep}$

$$6 \times 7 = 42 \text{ CNOTs}$$

$$5 \times 7 = 35 \text{ single-qubit gates}$$

$$3 \times 7 = 21 \text{ units}$$

$$6 \times 7 = 42 \text{ measurements}$$

$$6 \text{ preparations}$$

$$B = 140 \cdot 6C, \text{ combinations } 107 \text{ prep}$$

$$C = 21$$

Prob. (multiple bad erRec) - not independent



3 physical errors, but 2 bad erRecs

Truncation: Starting from end of FT circuit, truncated
any erRec that is followed by a bad erRec. If the
truncated erRec is good, it counts as good for further truncations.
Now prob. (multiple bad erRecs) \leq IT prob. (each bad)

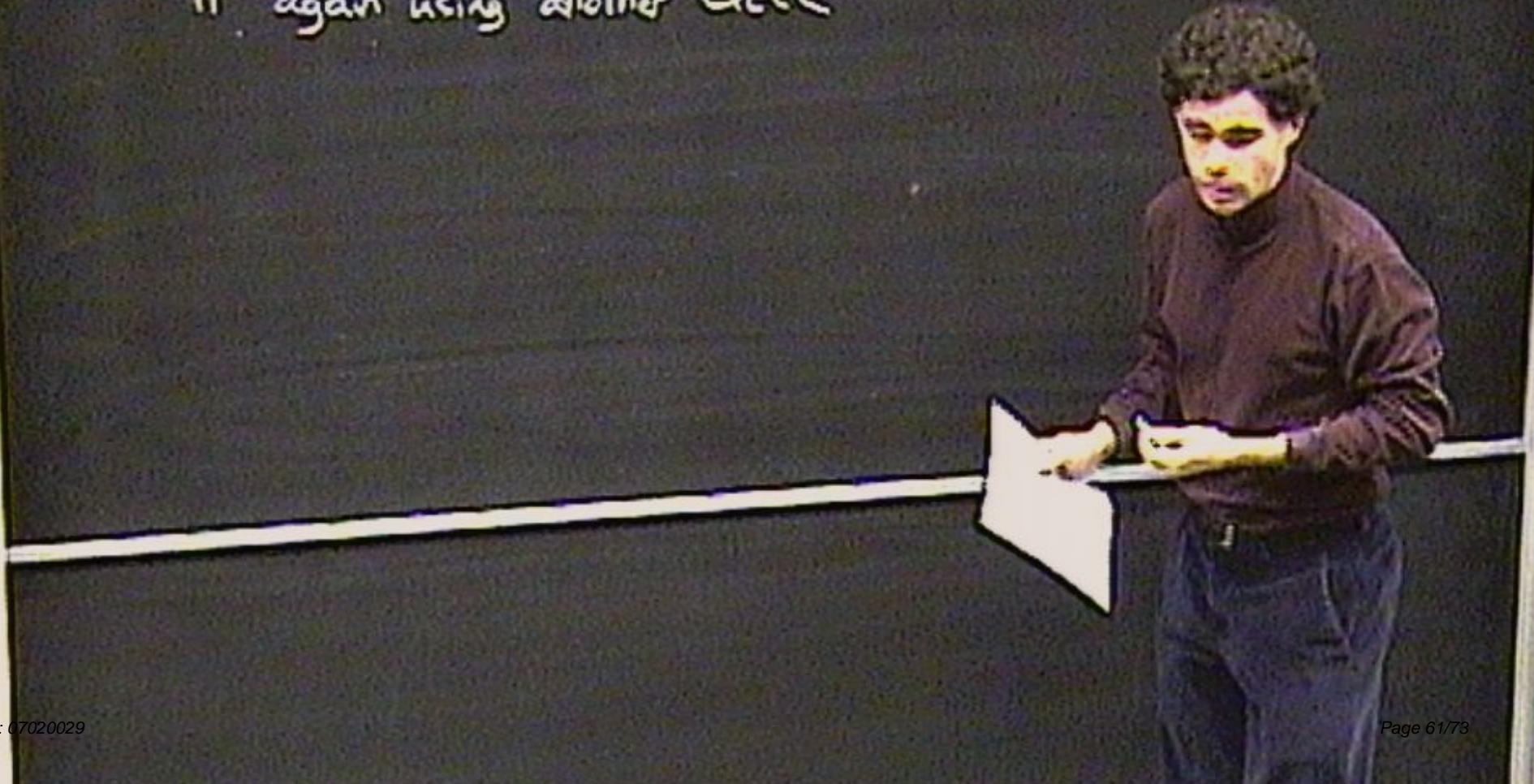
Thm (Local reduction): A FT circuit can be replaced by a noisy
enclosed circuit, with errors bounded by prob $p' = \left(\frac{A}{n}\right)p^{tn}$, where A is
the number of locations in the largest erRec.

$$T=1: P' = \left(\frac{A}{Z}\right) P^2, \quad P_T = \frac{1}{\sqrt{2}} \Rightarrow P' = P_T \left(\frac{P}{P_T}\right)^2$$



$$T=1: P' = \left(\frac{A}{Z}\right) P^2, \quad P_T = \frac{1}{P} \Rightarrow P' = P_T \left(\frac{P}{P_T}\right)^2 = P_T \left(\frac{P}{P_T}\right)$$

Concatenation: Take each qubit of a QECC and encode it again using another QECC



$$T=1: P' = \begin{pmatrix} A \\ z \end{pmatrix} P^2, \quad P_T = \frac{1}{2} \rightarrow P' = P_T \left(\frac{P}{P_T} \right)^2 = P_T (P_{FT})$$

Concatenation: Take each qubit of a QECC and encode it again using another QECC. Take a FT circuit, treat it as a circuit of physical gates - make it FT again.

$$T=1: P' = \begin{pmatrix} A \\ z \end{pmatrix} P^2, \quad P_T = \frac{1}{P} \Rightarrow P' = P_T \left(\frac{P}{P_T} \right)^2 = P_T \left(\frac{P}{P_T} \right)$$

Concatenation: Take each qubit of a QECC and encode it again using another QECC. Take a FT circuit, treat it as a circuit of physical gates - make it FT again. Each time we do this, it adds one level of concatenation. Level 0 = physical qubits, top level = logical qubits.

Thm [Threshold th]: There exists a threshold P_T such that
if the error rate per location $p < P_T$

Thm [Threshold th]: There exists a threshold p_T such that if the error rate per location $p < p_T$, then arbitrarily long computations are possible. To achieve error rate ϵ per logical location (say $\epsilon \gg \delta$), we need overhead $\text{polylog } \epsilon$. (overhead = mult. plus
blump in # qubits)

Thm [Threshold th]: There exists a threshold p_T such that if the error rate per location $p < p_T$, then arbitrarily long computations are possible. To achieve error rate ϵ per logical location (say $\epsilon \gg 0$), we need overhead $\text{polylog}^k \epsilon$. (overhead: multiplicative
blump is # qubits)

Proof:

Thm [Threshold th]: There exists a threshold p_T such that if the error rate per location $p < p_T$, then arbitrarily long computations are possible. To achieve error rate ϵ per logical location (say $\epsilon \gg \alpha$), we need overhead $\text{polylog}^{1/\epsilon}$. (overhead = multi-plaquette
blump in # qubits)

Proof: Apply local reduction repeatedly to a corrected FT circuit

Thm [Threshold-thr]: There exists a threshold p_T such that if the error rate per location $p < p_T$, then arbitrarily long computations are possible. To achieve error rate ϵ per logical location (say $\epsilon > 0$), we need overhead $\text{polylog}^k \epsilon$. (overhead: multiplicative bump in # qubits)

Proof: Apply local reduction repeatedly to a corrected FT circuit

Error rate after running j levels

$$p_j = p_T \left(\frac{p_{T'} / p_T}{p_T} \right)^j = p_T \left(\frac{p_{T'} / p_T}{p_T} \right)^j = p_T \left(\frac{p_{T'}}{p_T} \right)^j$$

$$\text{To get } p_j = \epsilon, \text{ and } j = \frac{\log \epsilon / p_T}{\log p_{T'}/p_T} \Rightarrow j = \log \log \frac{\epsilon / p_T}{\log p_{T'}/p_T}$$

Thm [Threshold th]: There exists a threshold p_T such that if the error rate per location $p < p_T$, then arbitrarily long computations are possible. To achieve error rate ϵ per logical location (say $\epsilon > 0$), we need overhead $\text{polylog}^k \epsilon$. (overhead = multi-plaquette bloop is # qubits)

Proof: Apply local reduction repeatedly to a code word.

Error rate after running j loops

$$p_j = p_T \left(\frac{p_{j-1}}{p_T} \right)^j = p_T \left(\frac{p_0}{p_T} \right)^j = p_T \left(\frac{p}{p_T} \right)^j$$

$$\text{To get } p_j = \epsilon, \text{ need } j = \frac{\log \epsilon / p_T}{\log p_0 / p_T} \Rightarrow j = \log \log \frac{p}{\epsilon}$$

$$\text{Overhead } N^2 = \text{poly}(\log^2 \epsilon)$$

Thm [Threshold th]: There exists a threshold p_T such that if the error rate per location $p < p_T$, then arbitrarily long computations are possible. To achieve error rate ϵ per logical location (say $\epsilon > 0$), we need overhead $\text{polylog}^k \epsilon$. (overhead: multiplicative
blump in # qubits)

Proof: Apply local reduction repeatedly to a corrected FT circuit

$$\text{Error rate after running } j \text{ levels} \\ p_j = p_T \left(\frac{p_{j+1}}{p_T} \right)^j = p_T \left(\frac{p_{j+1}}{p_T} \right)^{\tilde{j}} = p_T \left(\frac{p}{p_T} \right)^{\tilde{j}}$$

$$\text{To get } p_j = \epsilon, \text{ need } \tilde{j} = \frac{\log(p/p_T)}{\log(p_T)} \Rightarrow j = \log \log(p/\epsilon) - \log \log(p_T)$$

$$\text{Overhead } N^2 = \text{poly}(\log(1/\epsilon))$$

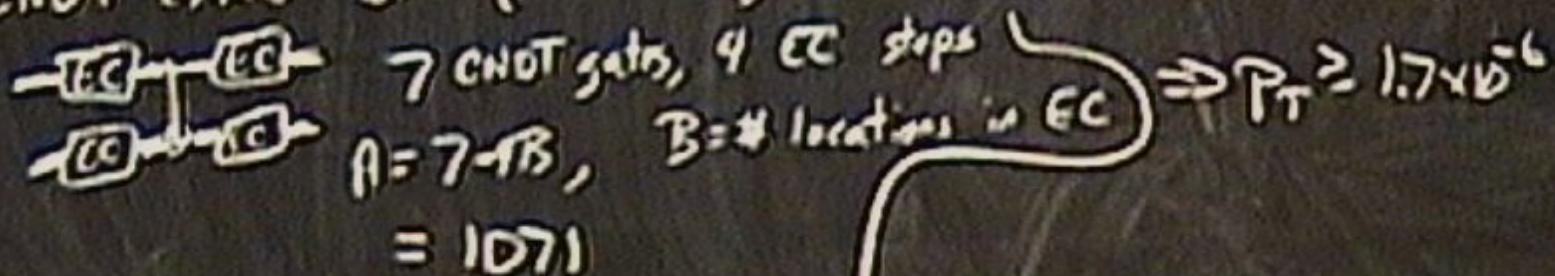
What is the probability of a bad exRec?

Need $t+1$ bad locations, $\binom{t+1}{A}$ of having errors in a particular set

There are $\binom{A}{t+1}$ sets, where $A = \#$ locations in exRec

$$P(\text{Bad}) \leq \binom{A}{t+1} p^{t+1}$$

E.g.: CNOT exRec for 7-qubit code, $t=1$ $P(\text{Bad}) \leq \binom{A}{2} p^2 = (572,985) p^2$


7 CNOT gates, 4 CC steps
 $A = 7 - tB$, $B = \# \text{locations in EC}$ $\Rightarrow P_T \geq 1.7 \times 10^{-6}$
 $= 1071$

$$P_{ij} = P_T \left(\frac{P_i}{P_T} \right)^j = P_T \left(\frac{1 - \epsilon_j}{P_T} \right)^j = P_T \left(\frac{P}{P_T} \right)^j$$

To get $P_j = \epsilon_j$, need $j = \frac{\log \epsilon_j}{\log P_T} \Rightarrow j = \log \log \frac{P}{\epsilon_j} - \log \log P_T$

$$\text{Overhead } N^2 = \epsilon_{\text{bad}} (\log \%)$$

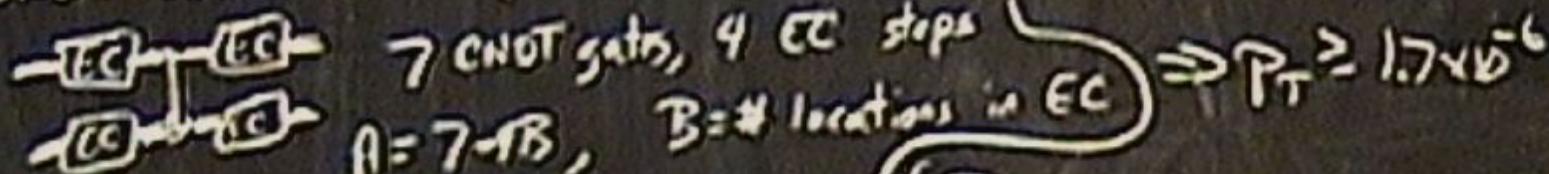
What is the probability of a bad error?

Need $t+1$ bad locations, \hat{P}^{t+1} of having errors in a particular set

There are $\binom{A}{t+1}$ sets, where $A = \#$ locations in error

$$P(\text{Bad}) \leq \binom{A}{t+1} p^{t+1}$$

E.g.: CNOT error for 7-qubit code, $t=1$



$$A = 7 - tB, \quad B = \# \text{ locations in EC}$$

$$= 1071$$

$$P(\text{Bad}) \leq \binom{A}{t+1} p^2 = (572,985) p^2$$

$$\Rightarrow P_T \geq 1.7 \times 10^{-6}$$

(Better thresholds:

For 7-qubit code, $P_T \geq 2.7 \times 10^{-6}$

Best proofs threshold $\sim 10^{-3}$

Best simulations: threshold $\sim 5-6\%$

$$P_{II} = P_T \left(\frac{P_e}{P_T} \right)^2 = P_T \left(10\% \right)^2 = P_T \left(\frac{P}{P_T} \right)^2$$

$$\text{To get } P_T = C, \text{ need } C = \frac{\log \epsilon_{\text{PT}}}{\log P_T} \Rightarrow j = \log \log \frac{1}{\epsilon_{\text{PT}}} - \log \log \frac{1}{P_T}$$

$$\text{Overhead } N^j = \log \left(\log \frac{1}{\epsilon_{\text{PT}}} \right)$$

What is the probability of a bad error?

Need $t+1$ bad locations, $\binom{t+1}{A}$ of having errors in a particular set

There are $\binom{A}{t+1}$ sets, where $A = \#$ locations in error

$$P(\text{Bad}) \leq \binom{A}{t+1} p^{t+1}$$

E.g.: CNOT error for 7-qubit code, $t=1$ $P(\text{Bad}) \leq \binom{A}{2} p^2 = (572,985) p^2$

$$\begin{array}{c} \text{---} \\ \text{[CNOT]} \\ \text{---} \end{array} \quad \begin{array}{c} \text{---} \\ \text{[CNOT]} \\ \text{---} \end{array}$$

7 CNOT gates, 4 EC steps

$A = 7 - tB$, $B = \#$ locations in EC

$$= 1071$$

$\Rightarrow P_T \geq 1.7 \times 10^{-6}$

(Better thresholds:

for 7-qubit code, $P_T \geq 2.7 \times 10^{-4}$

Best proofs threshold $\sim 10^{-3}$

Best simulations: threshold $\sim 5-6\%$

$$P_{ij} = P_T \left(\frac{p_i}{p_T} \right)^j = P_T \left(\frac{10\%}{p_T} \right)^j = P_T \left(\frac{p}{p_T} \right)^j$$

$$\text{To get } P_T = \epsilon, \text{ need } j = \frac{\log \epsilon / P_T}{\log p / p_T} \Rightarrow j = \log \log \frac{1/\epsilon}{p_T} - \log \log \frac{p}{p_T}$$

$$\text{Overhead } N^2 = \log_j (1/\epsilon)$$