Title: Quantum Error Correction 8A

Date: Feb 27, 2007 03:30 PM

URL: http://pirsa.org/07020028

Abstract: Assumptions for fault tolerance, extended rectangles, good, bad, and correct rectangles.

Assumptions used in constructing FT circuits:

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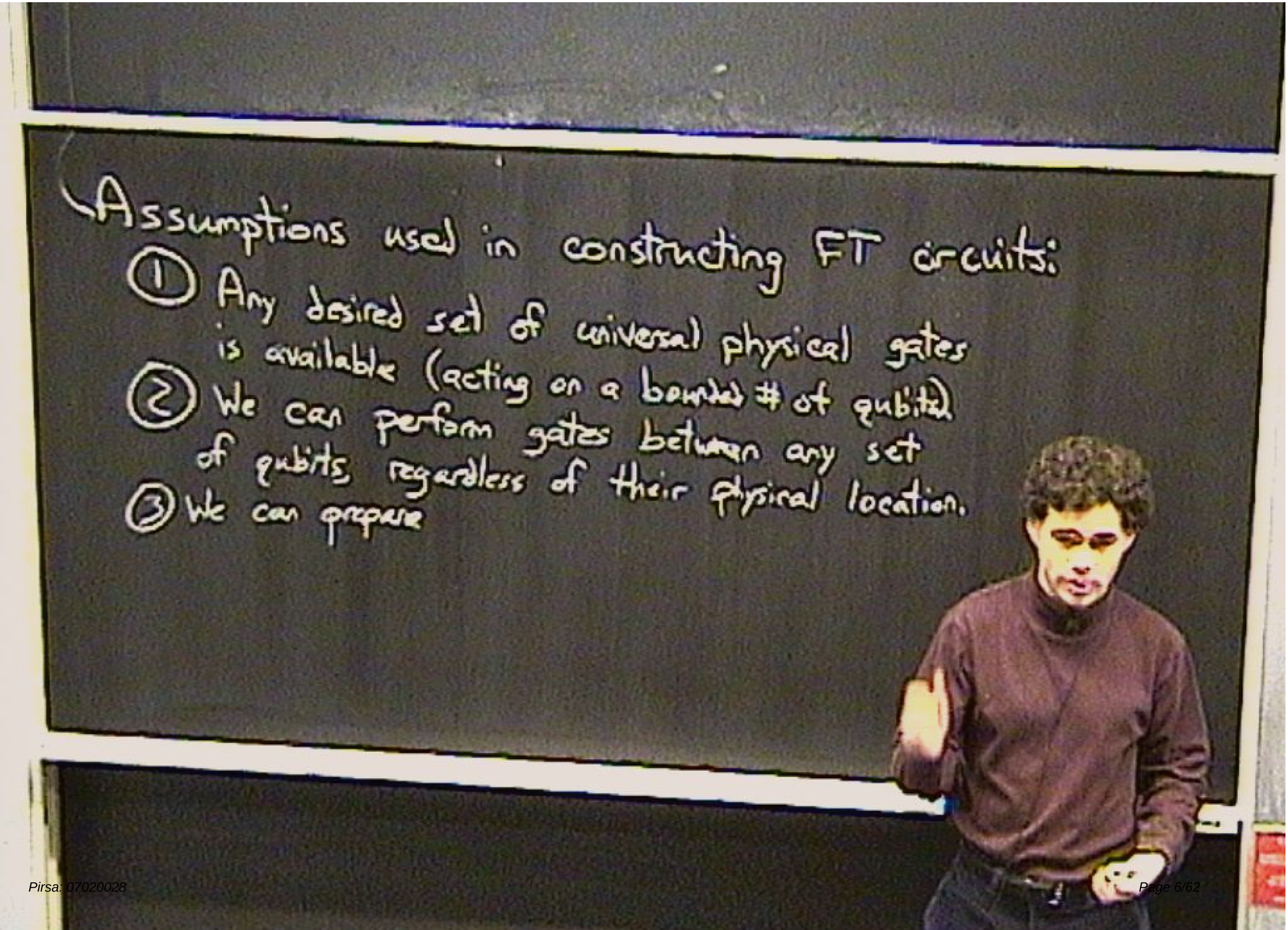
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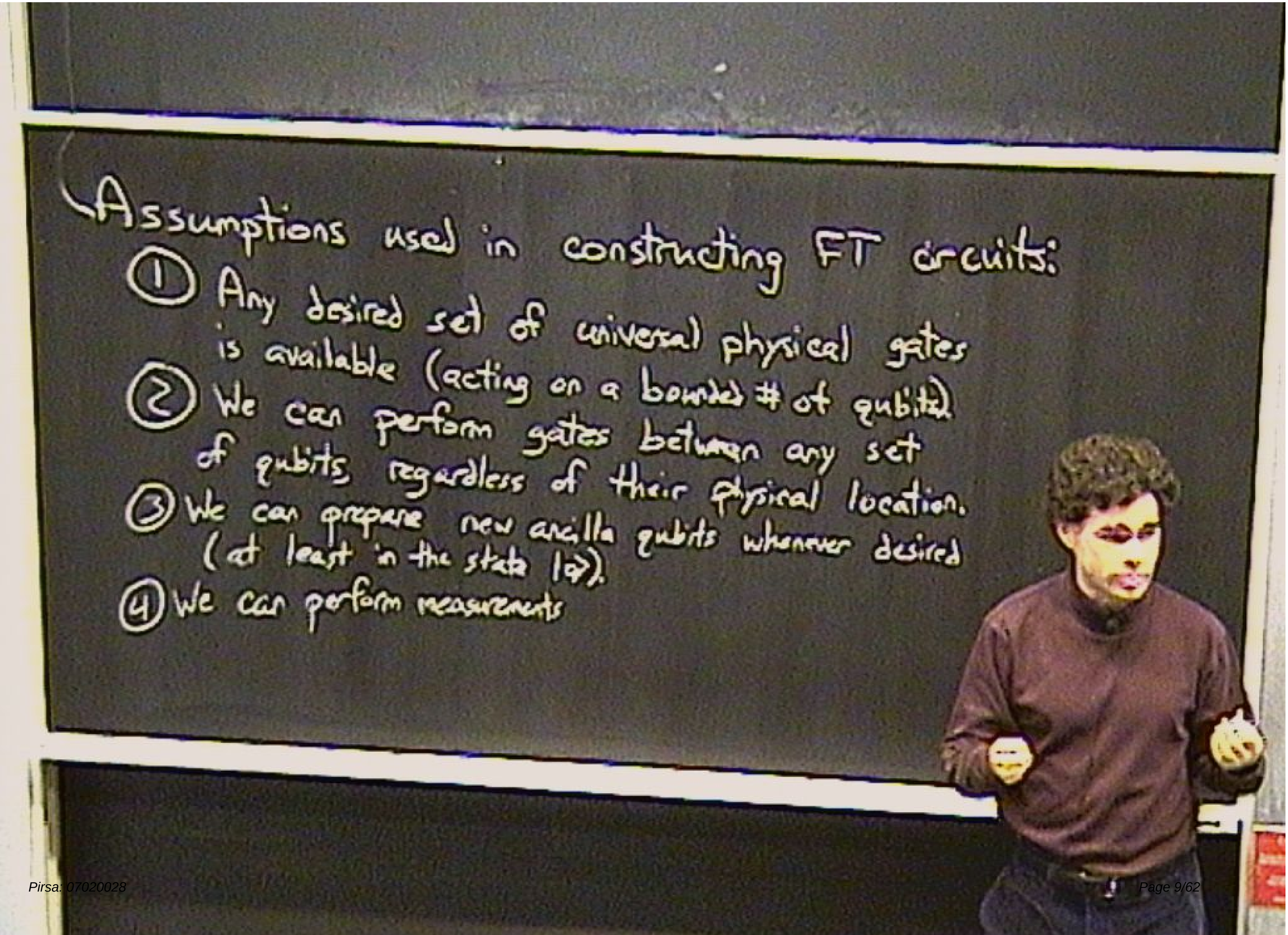
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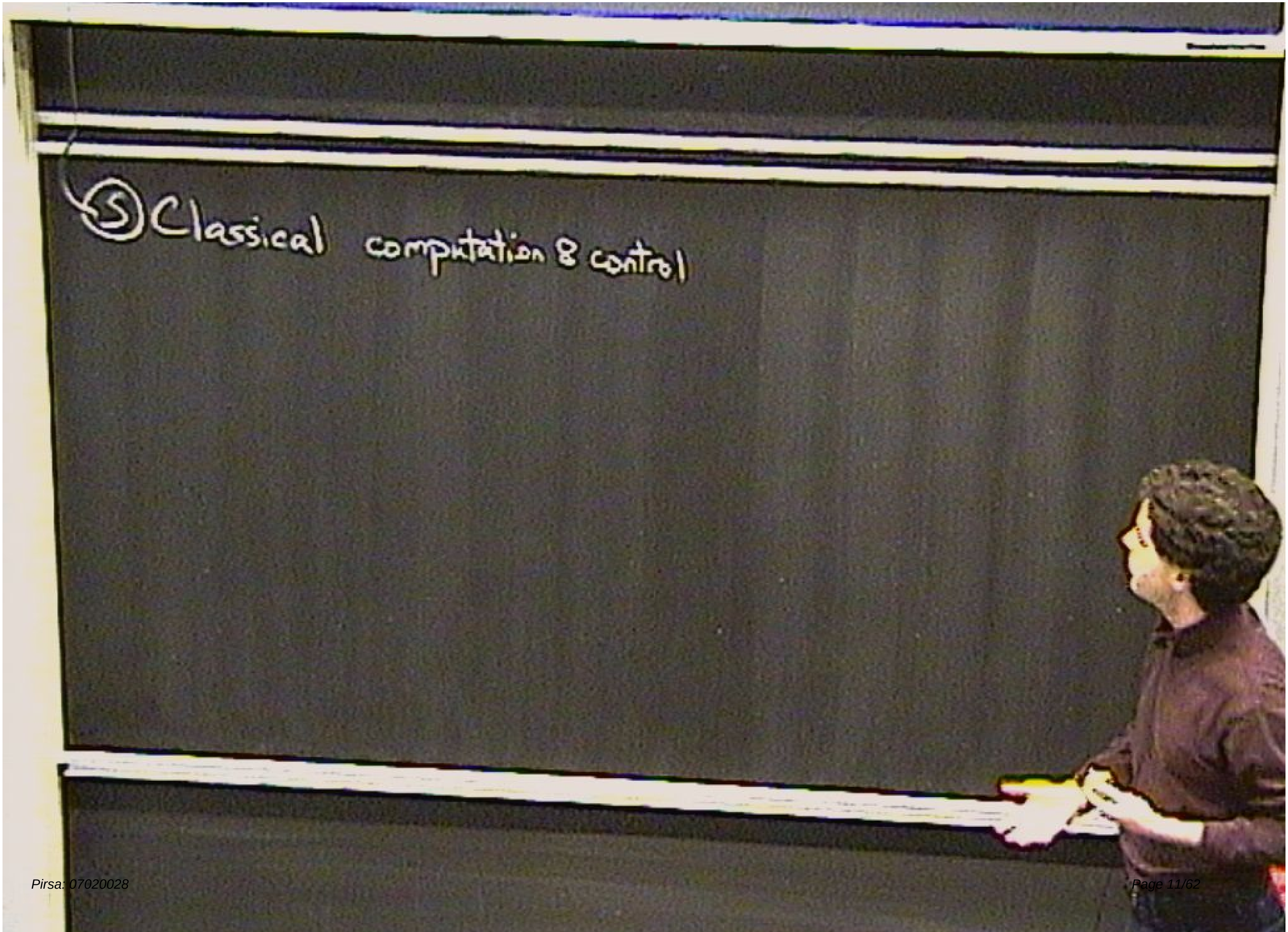
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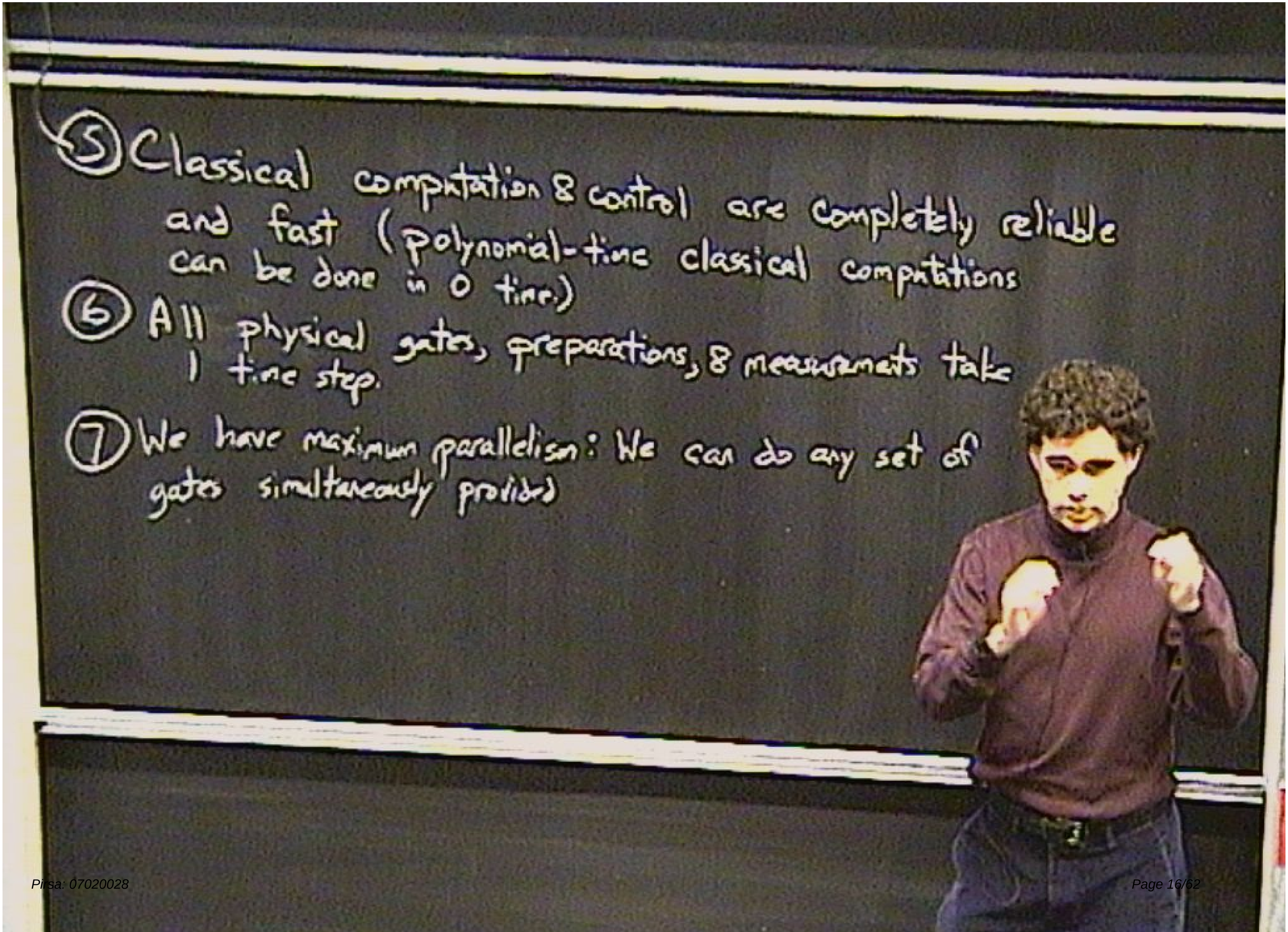
6. All physical gates, preparations, & measurements take 1 time step.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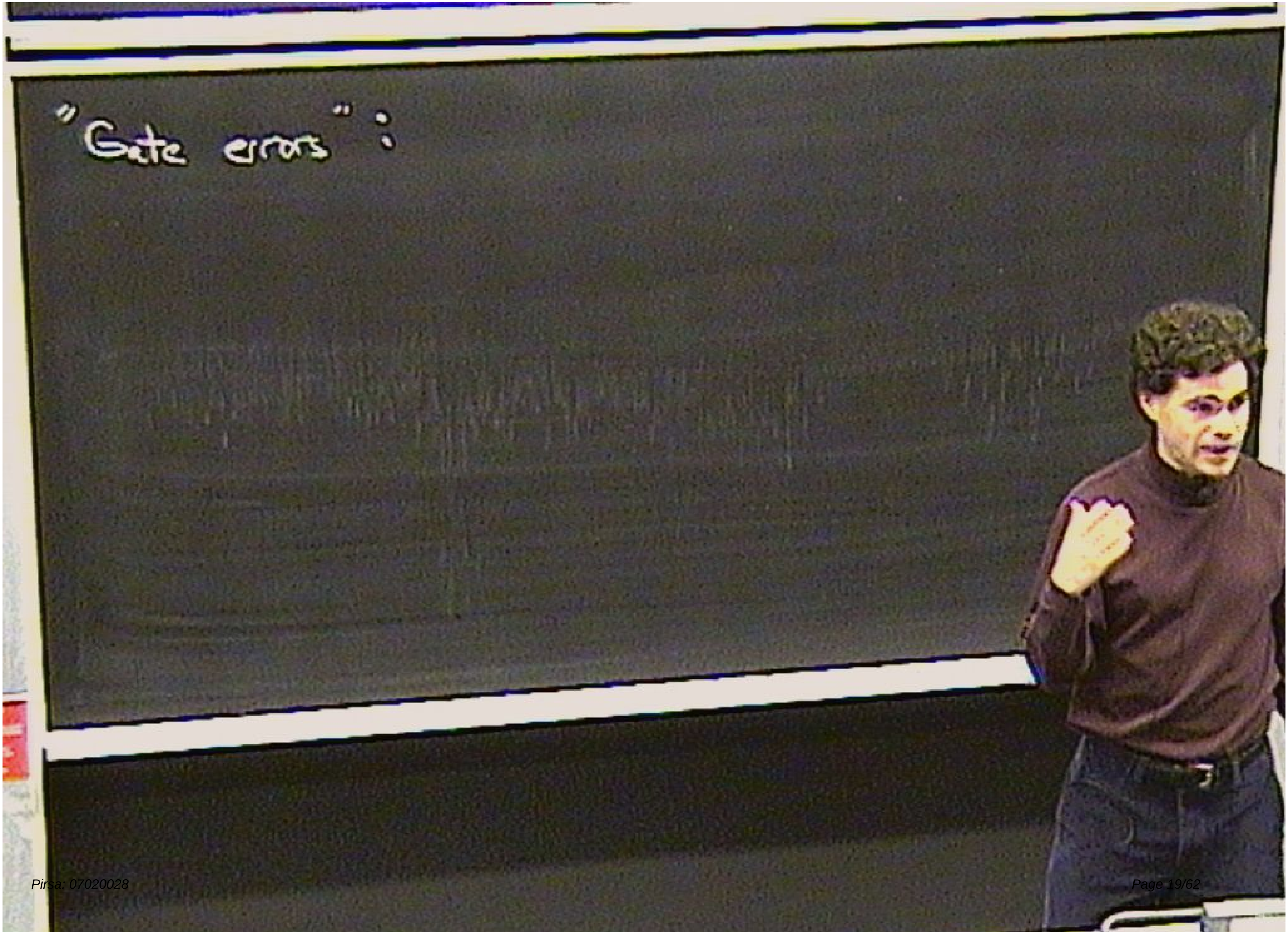
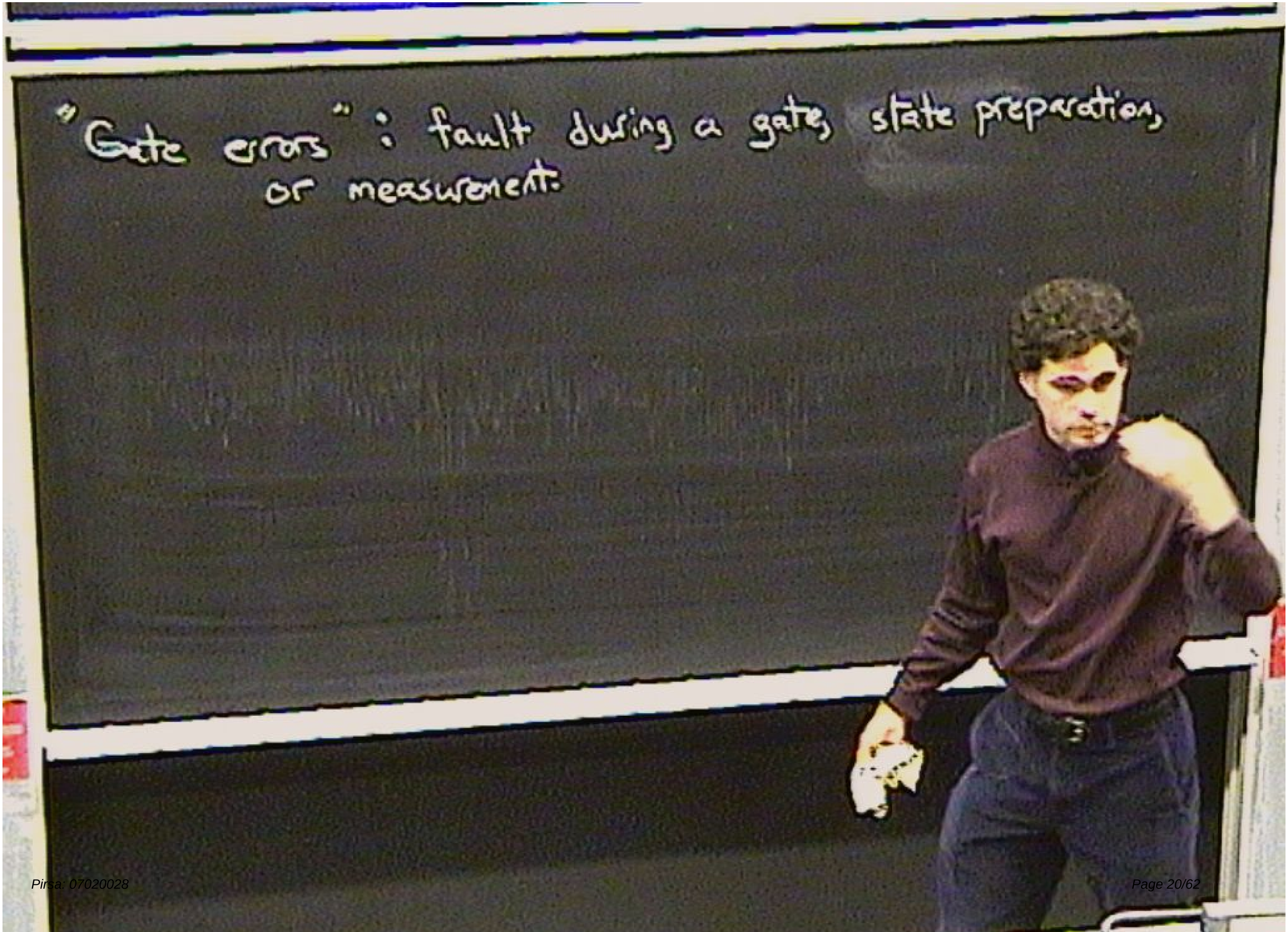

"Gate errors":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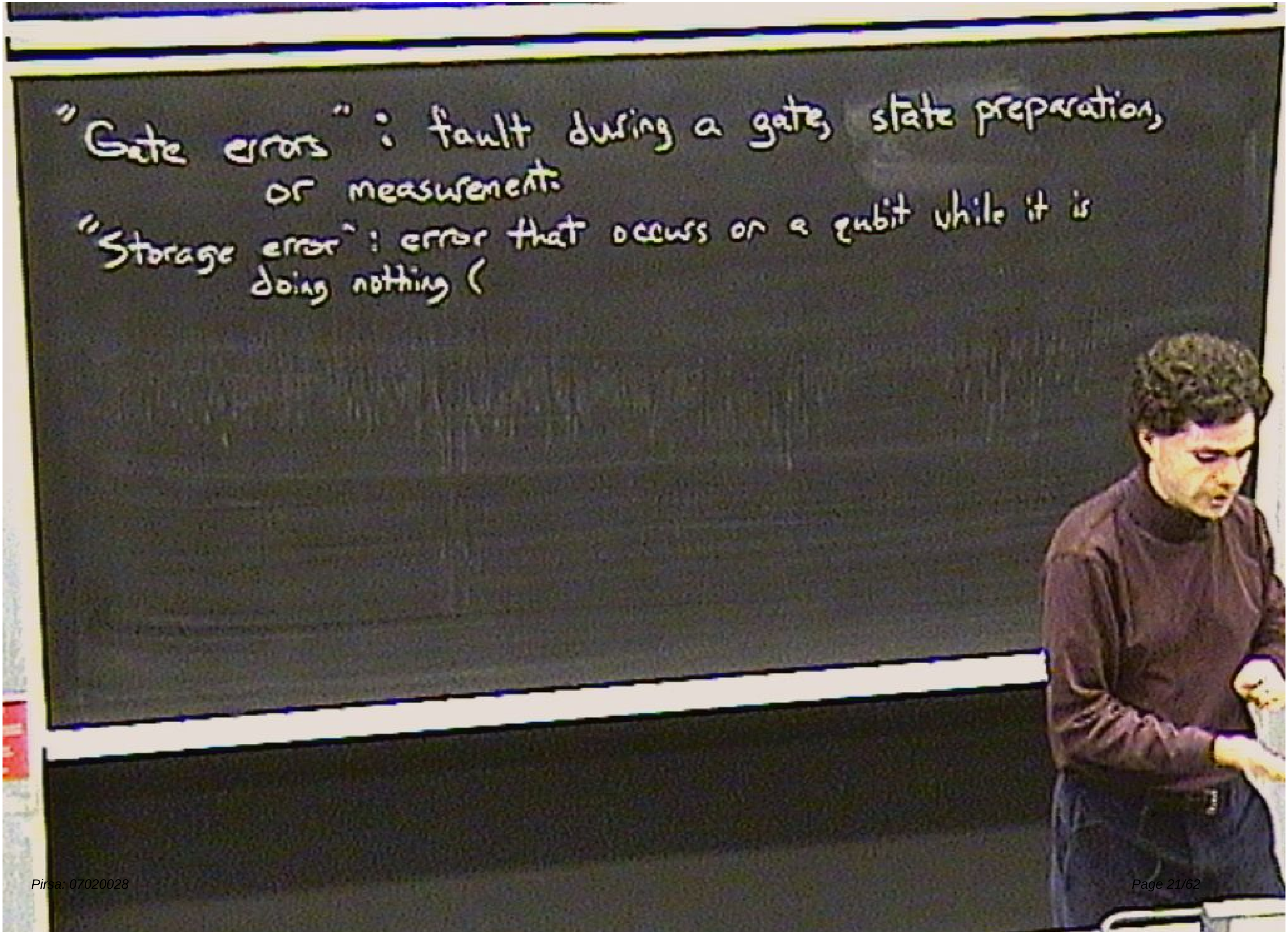
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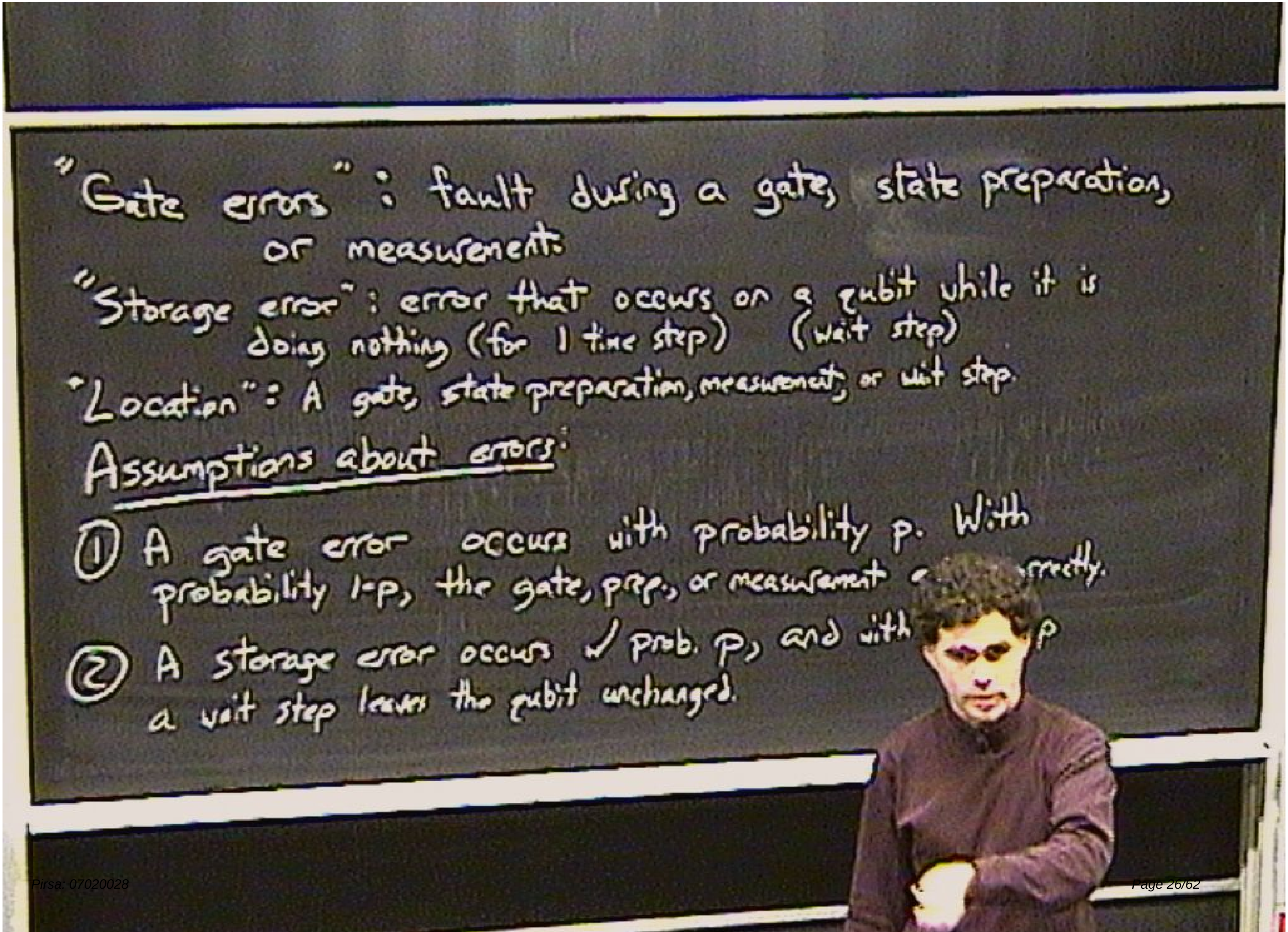
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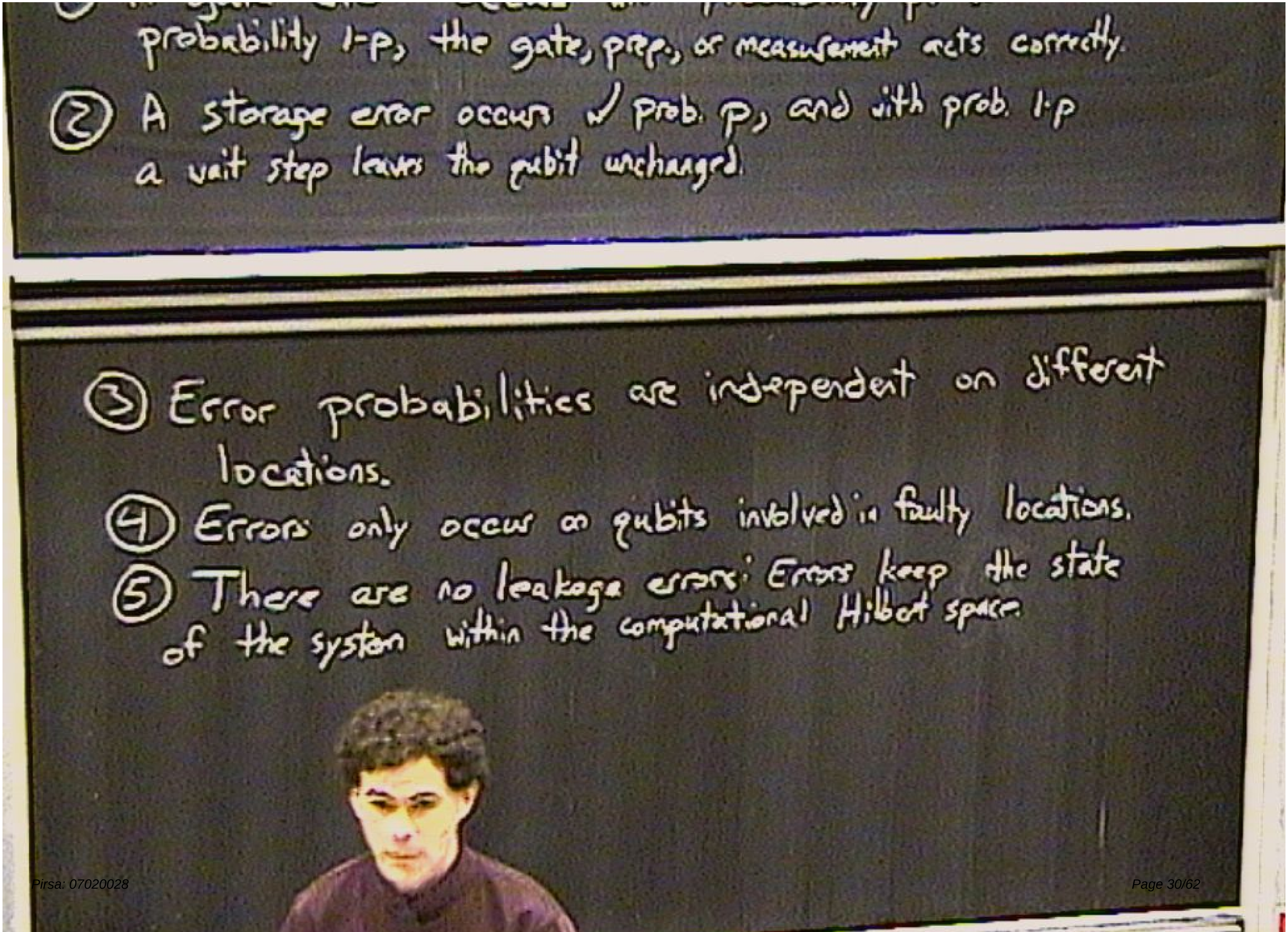
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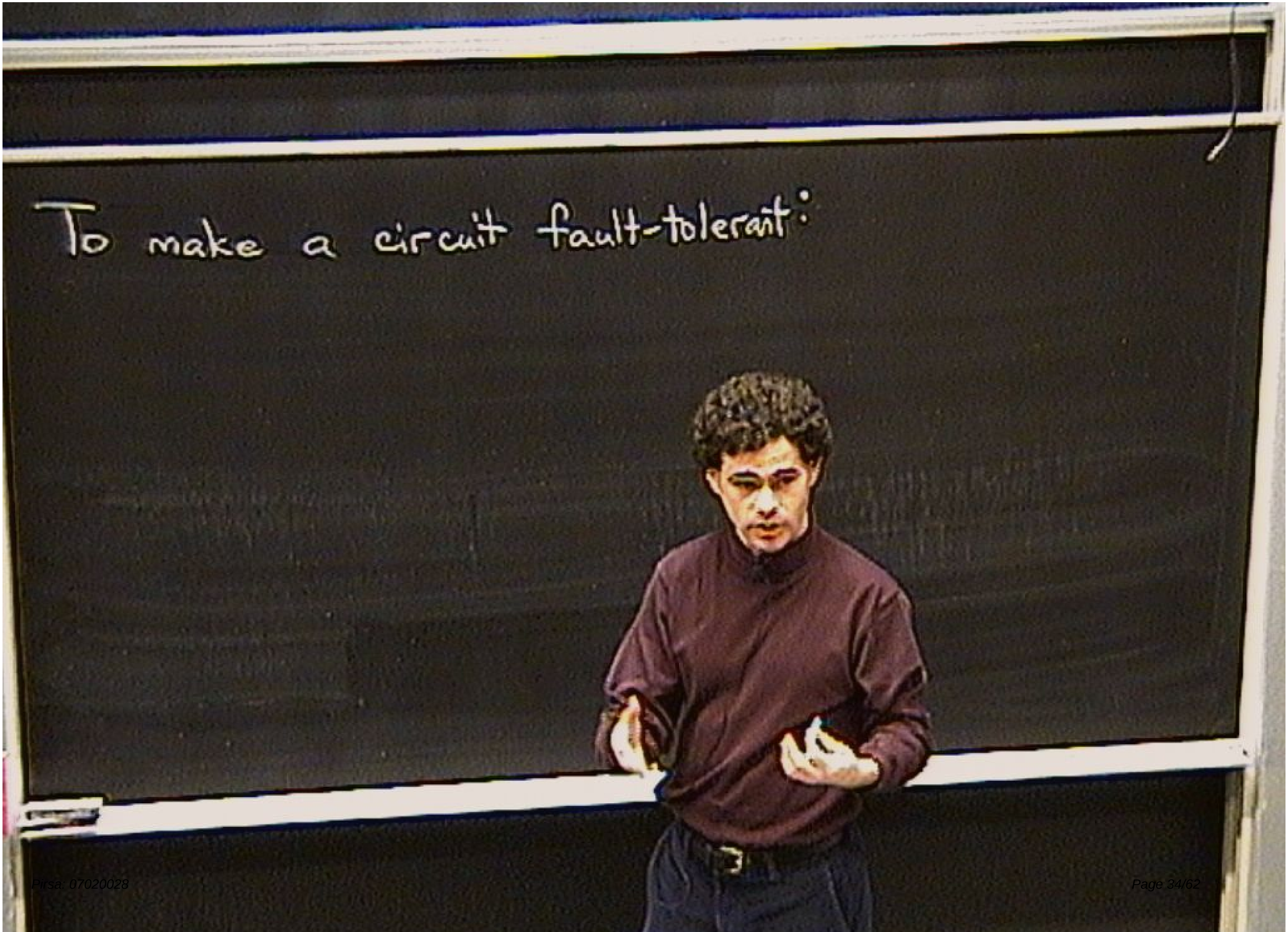
(6) Adversarial error model: Once the global locations of errors are selected, an adversary chooses a worst-case error for the faulty locations. This error is CPTP, but is otherwise unrestricted - e.g. may be a collective error between multiple faults, and might involve an ancilla held by the adversary.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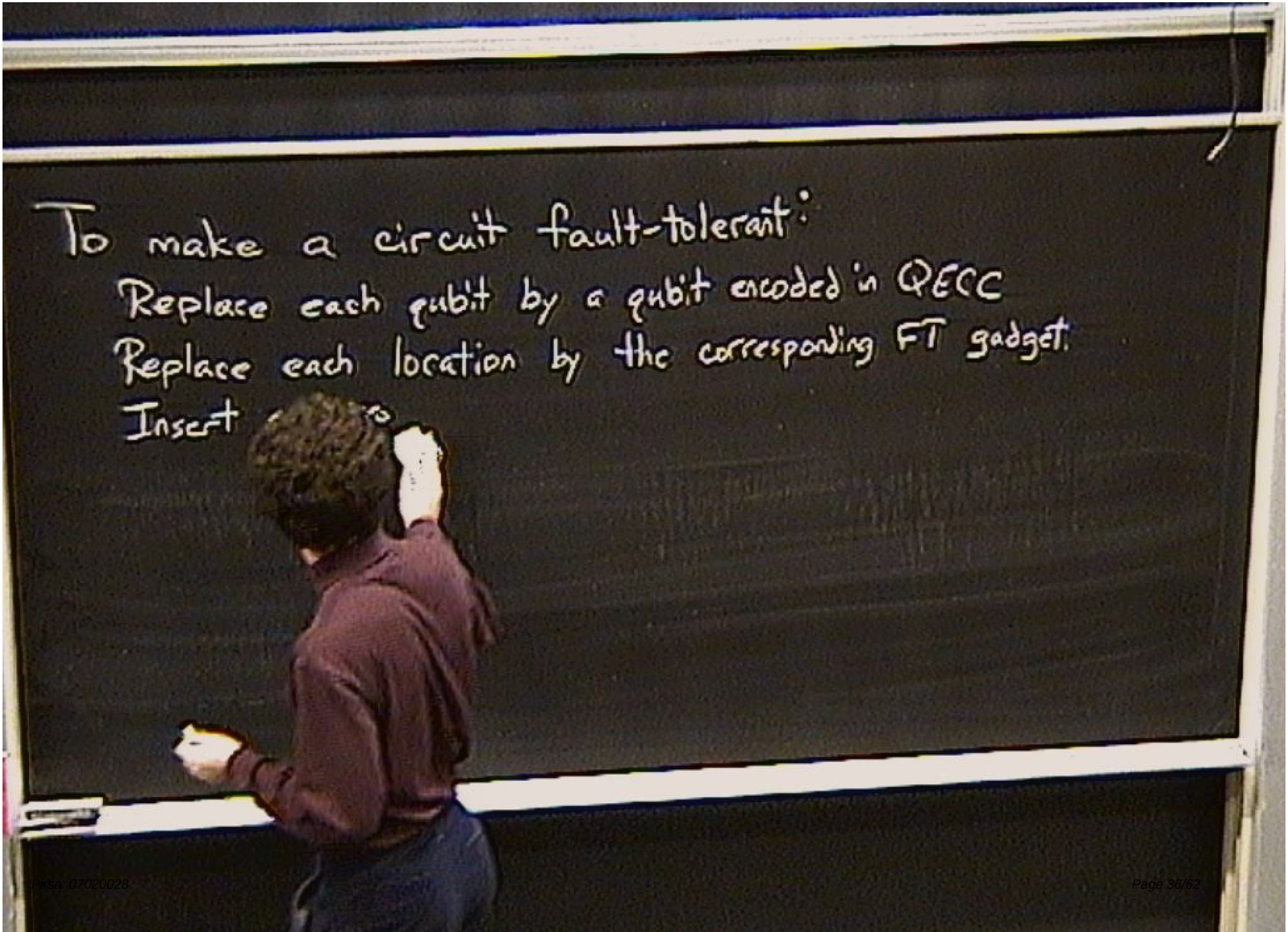
Replace each qubit by a qubit encoded in QECC

Replace each location by the corresponding FT gadget.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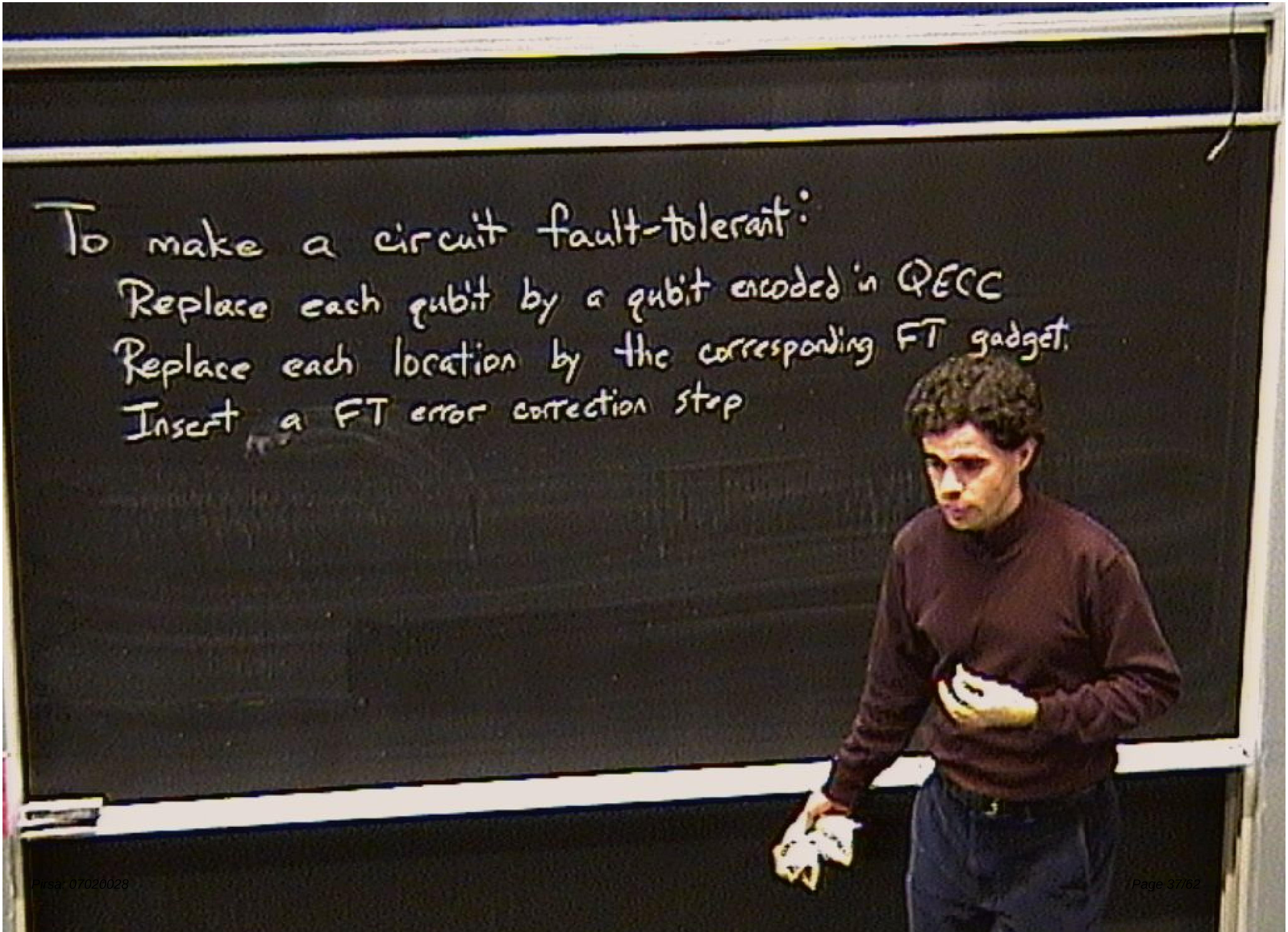
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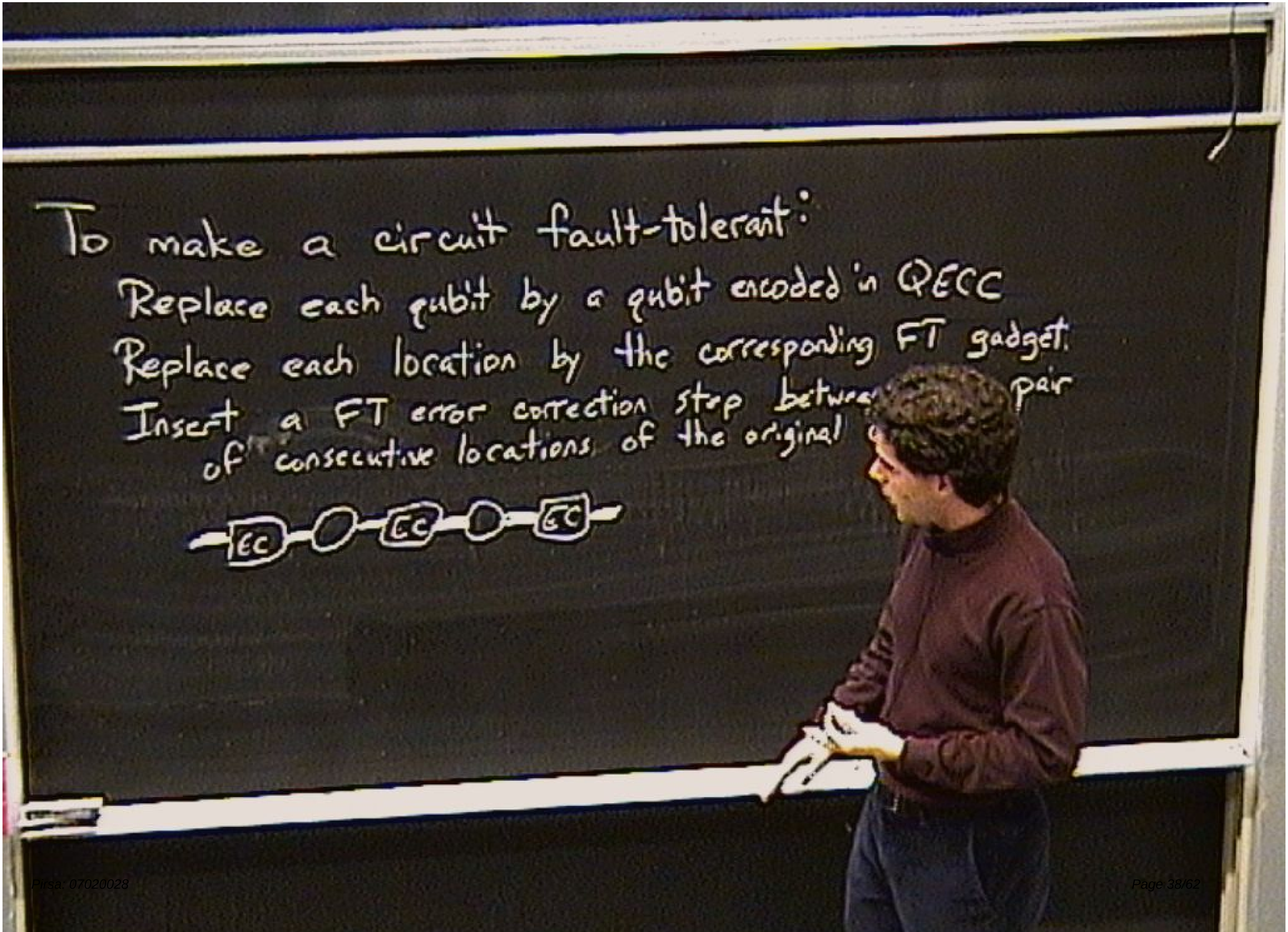
To make a circuit fault-tolerant:
Replace each qubit by a qubit encoded in QECC
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Insert a FT error correction step betwe
pair
of consecutive locations of the original
EC
EC
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To make a circuit fault-tolerant:

Replace each qubit by a qubit encoded in QECC

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Insert a FT error correction step between every pair of consecutive locations of the original circuit.

Extended rectangles

Each location in the original circuit corres[illegible] to an
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the EC steps before & after it.

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Extended rectangles overlap

Each location in the original circuit corresponds to an Extended Rectangle, consisting of the corresponding FT gadget plus the EC steps before & after it. (exRec = "extended rectangle")

The EC steps before & after it. (exRec = extended rectangle)

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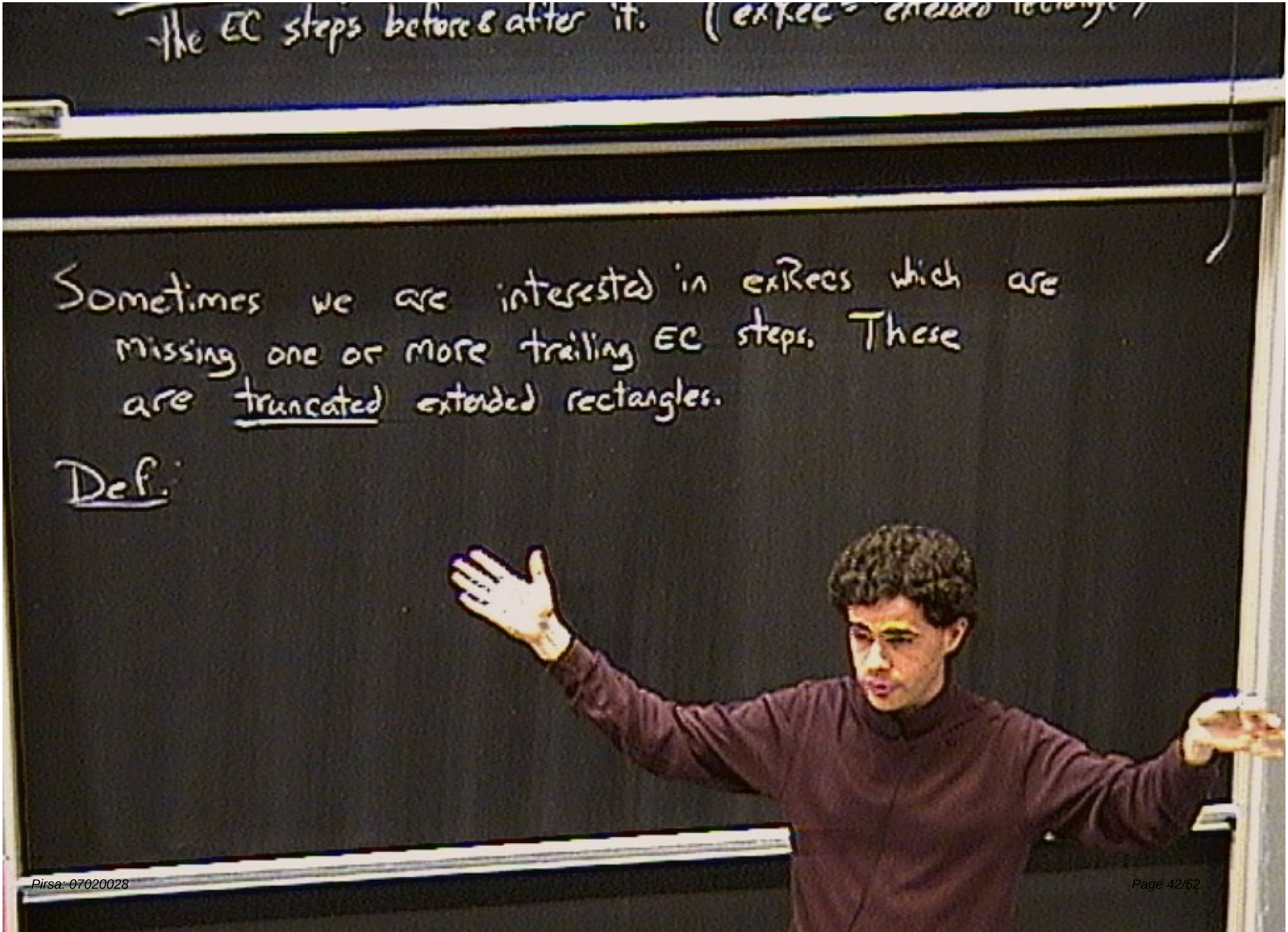
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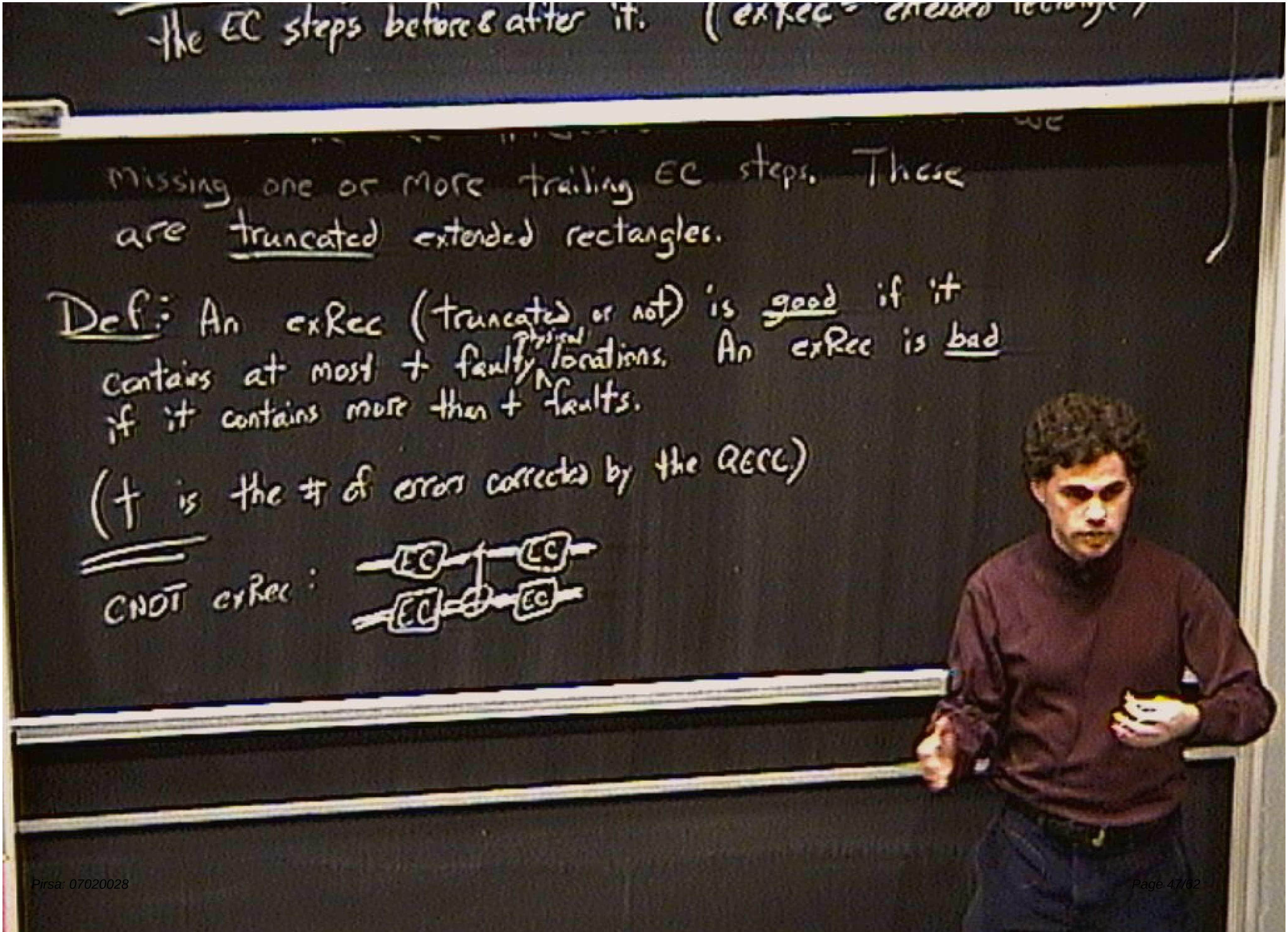
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CNOT exRec:
EC
EC
EC
EC

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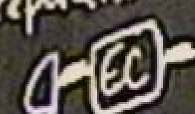
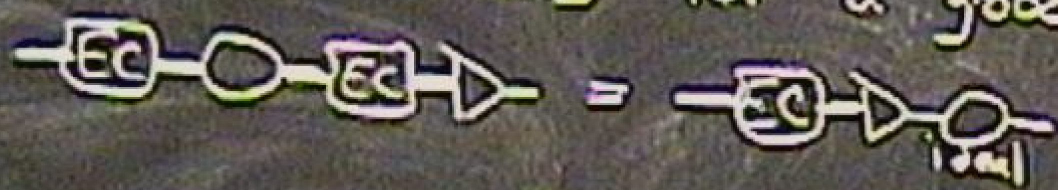
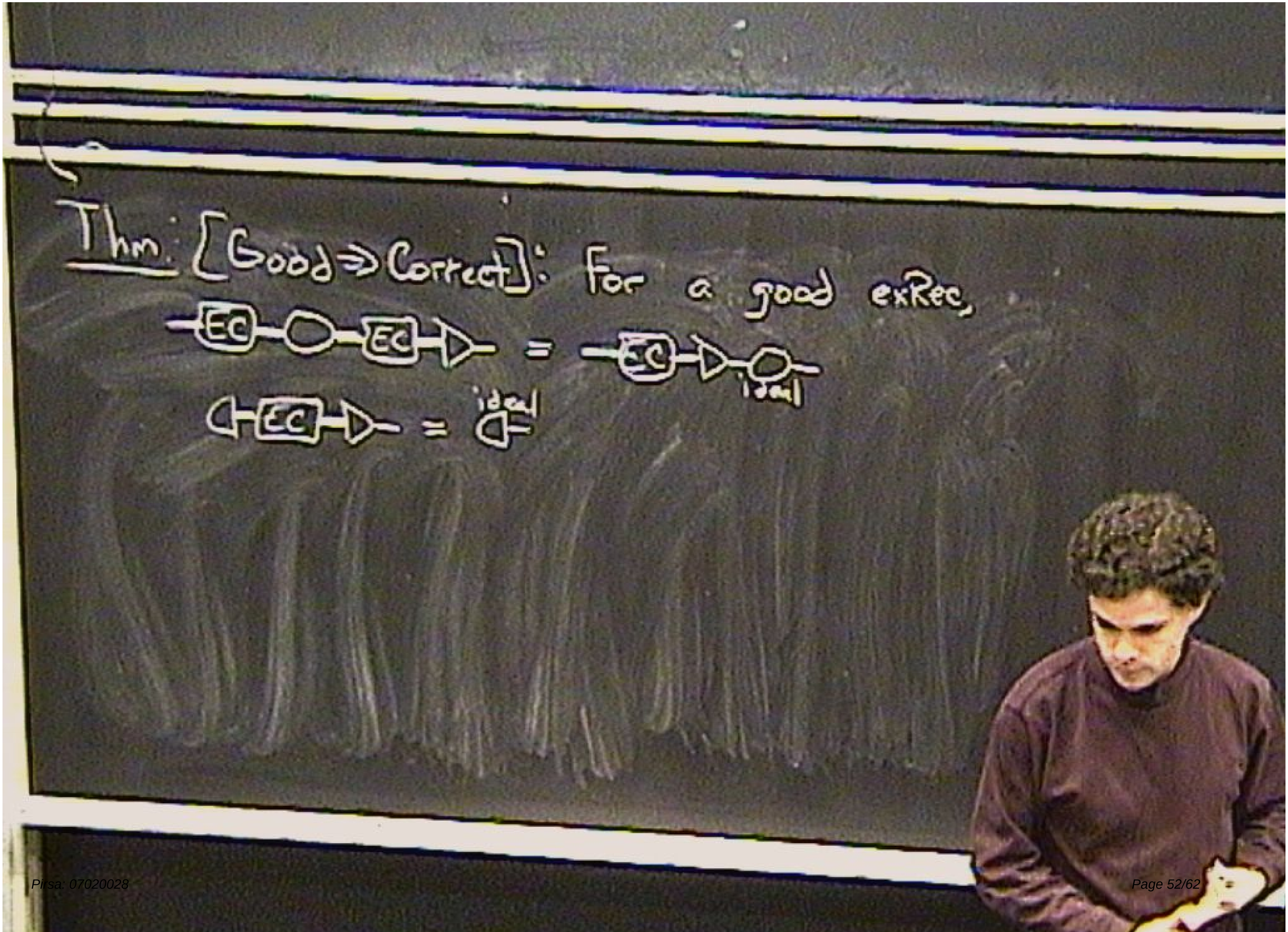


Measurement exRec:

<u>Thm:</u> [Good $\Rightarrow$ Correct]:

Thm: [Good ⇒ Correct]: For a good exRec,




Thm: [Good ⇒ Correct]: For a good exRec,
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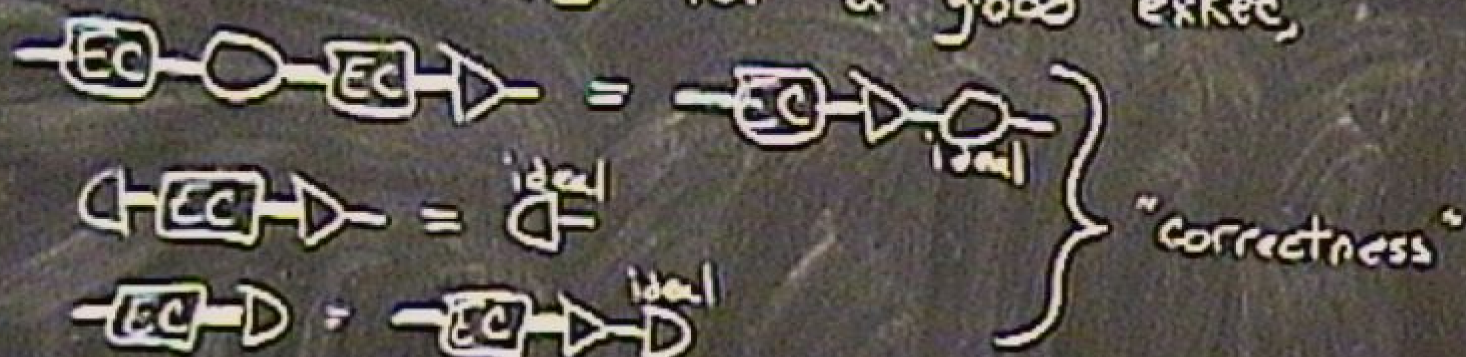

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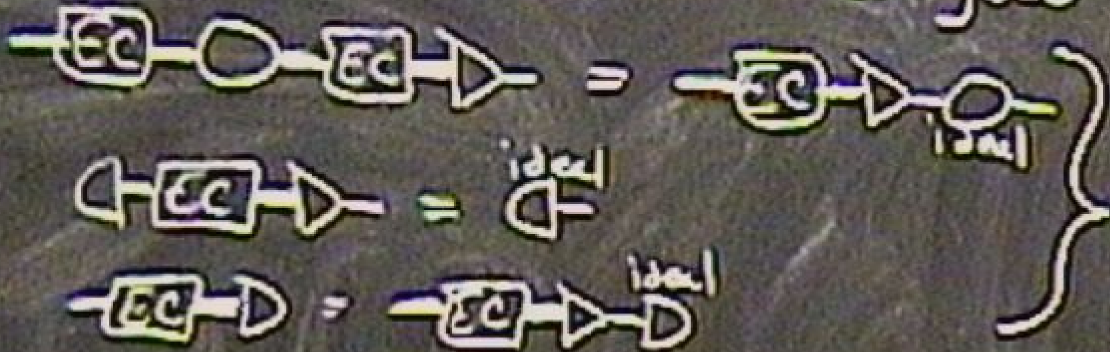
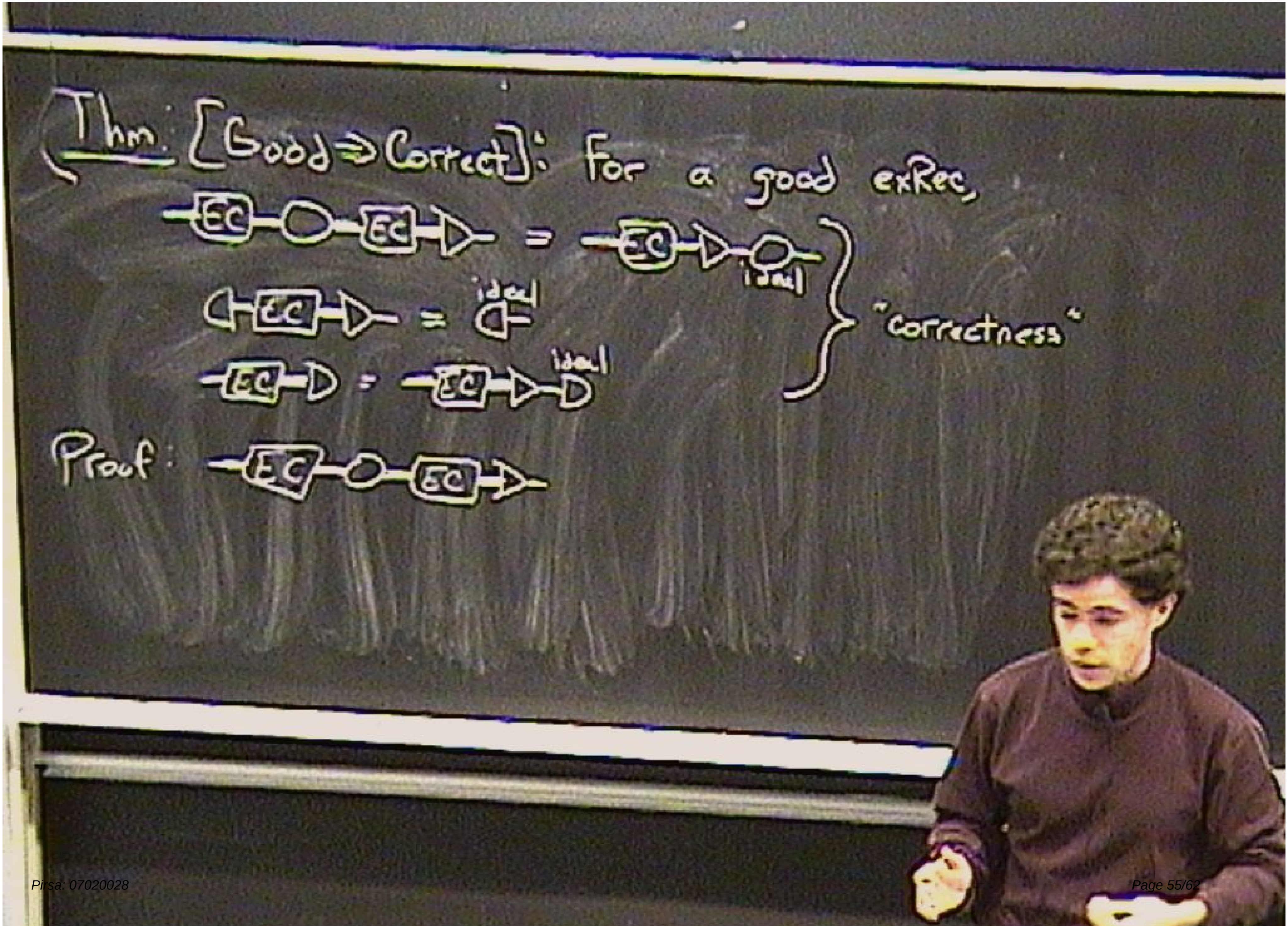


"correctness"

Proof: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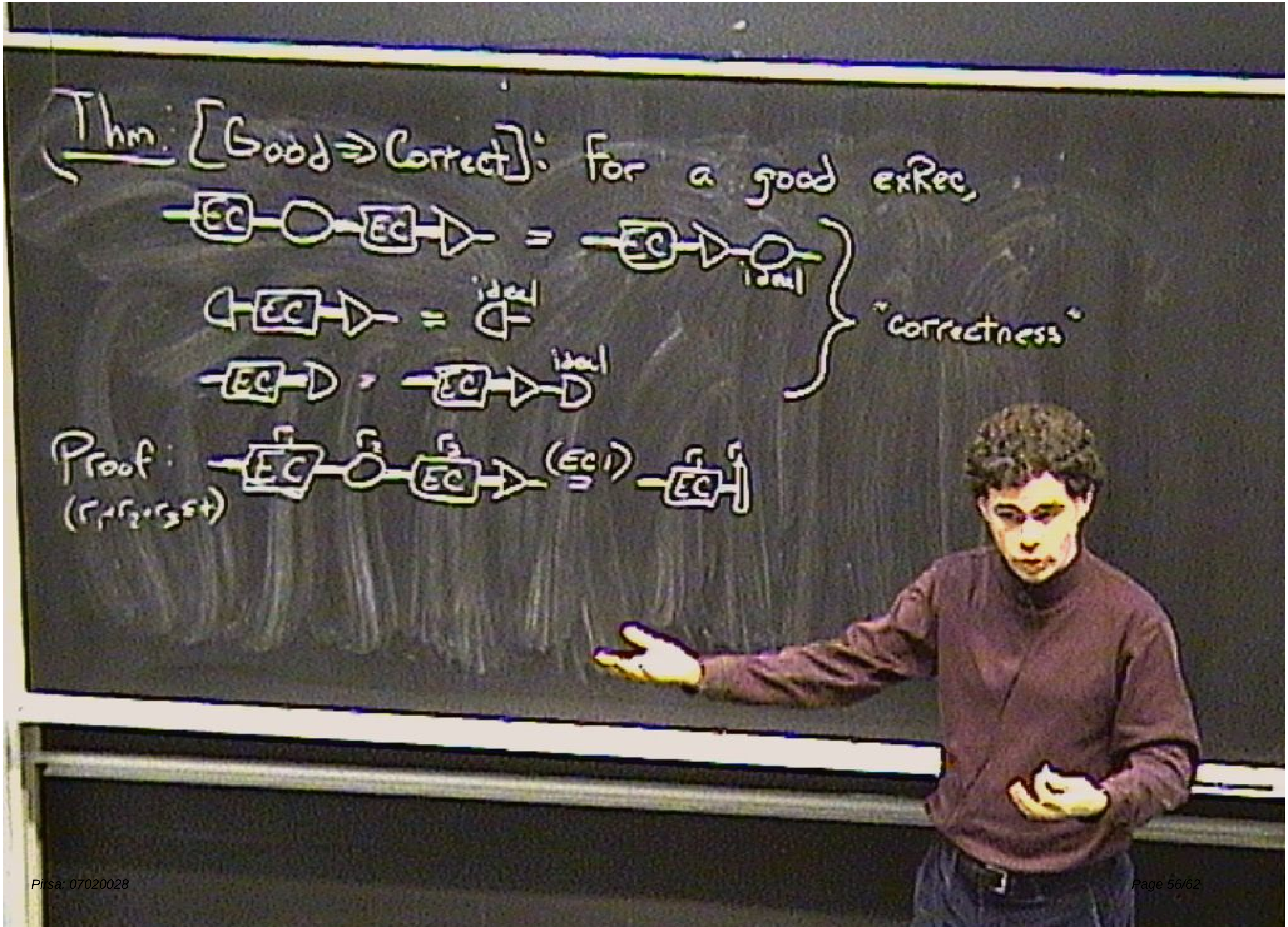
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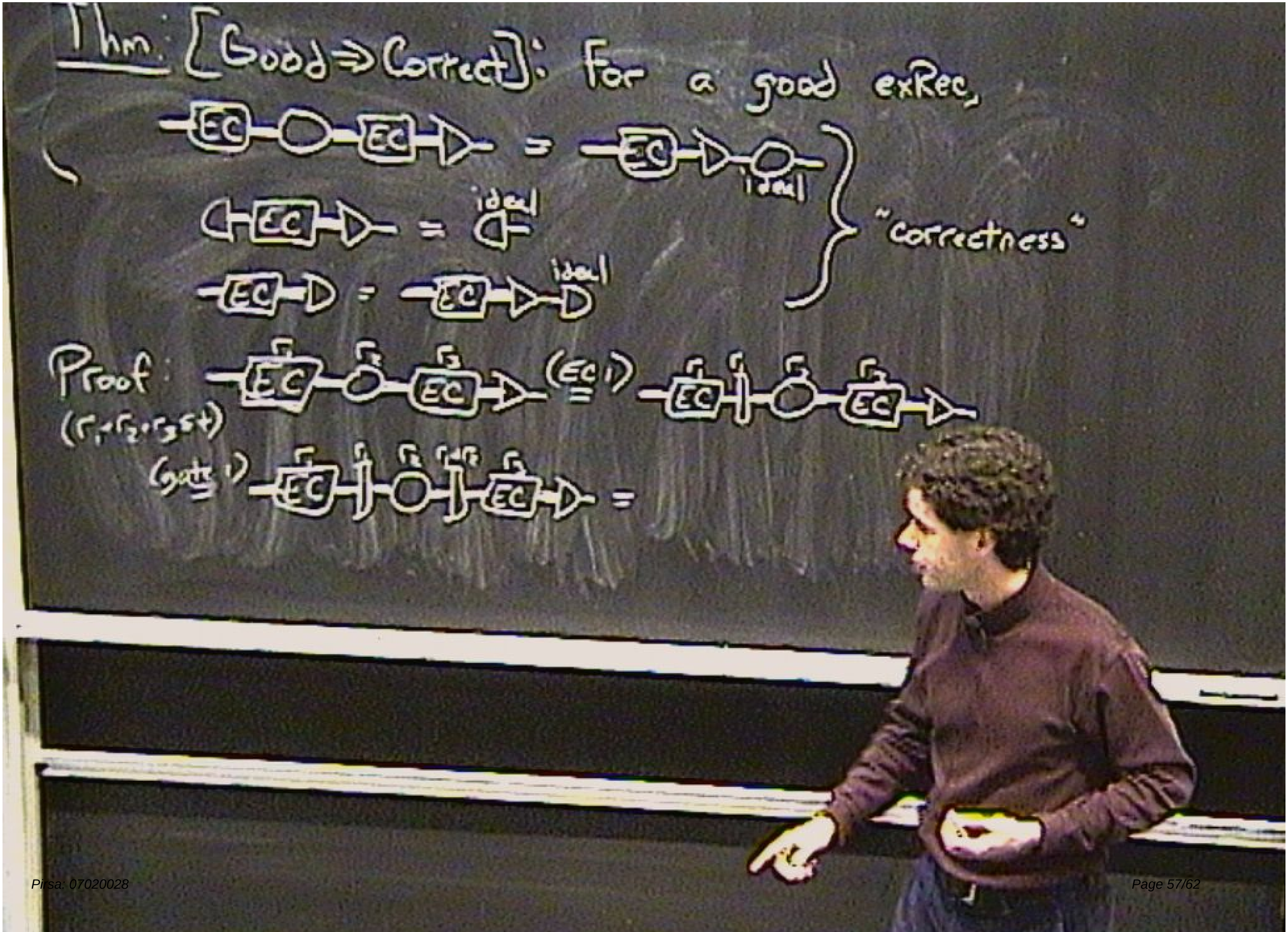
(r1+r2+r3≤t)
(EC1)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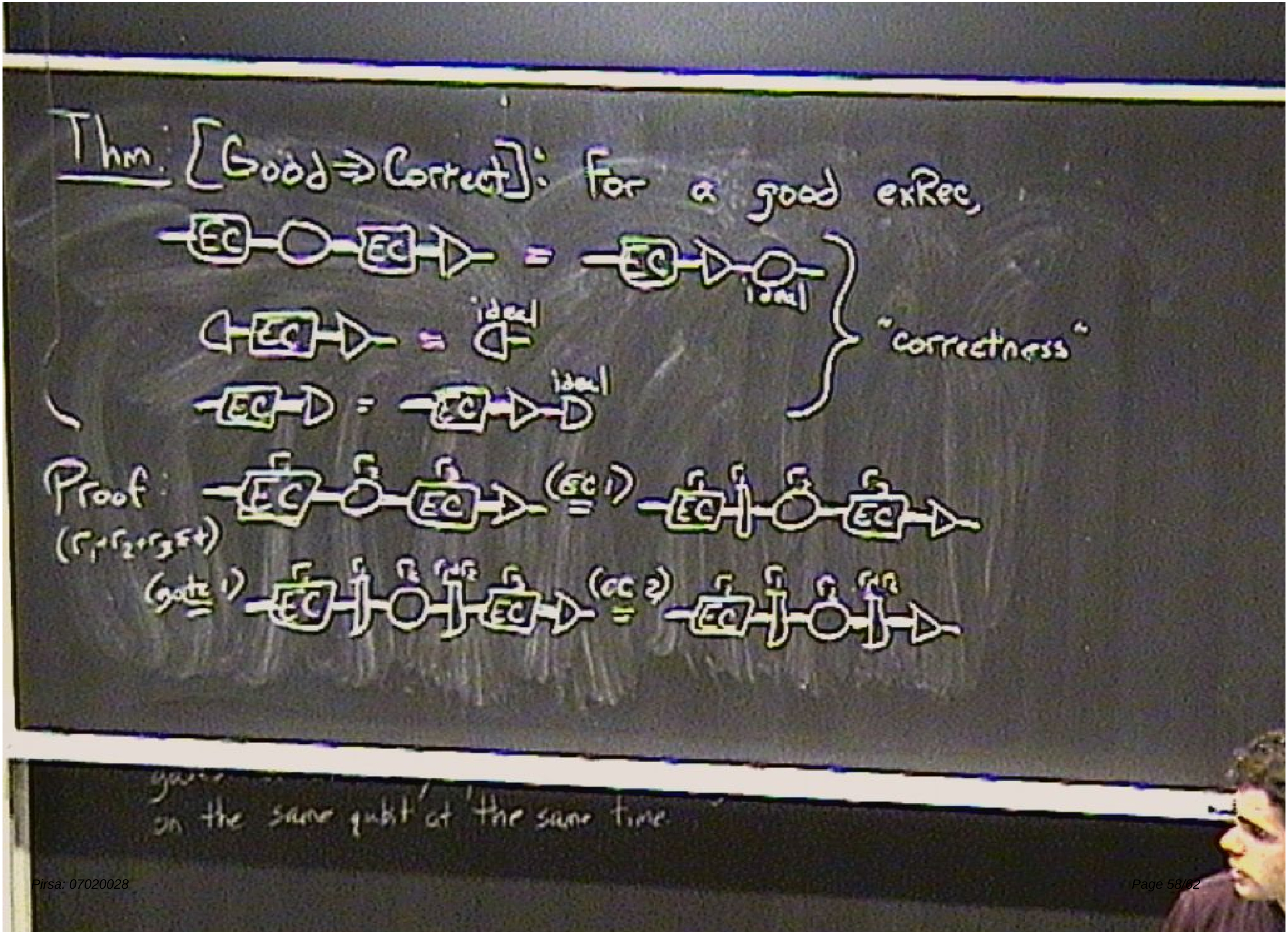
Thm: [Good ⇒ Correct]: For a good exRec,
ideal
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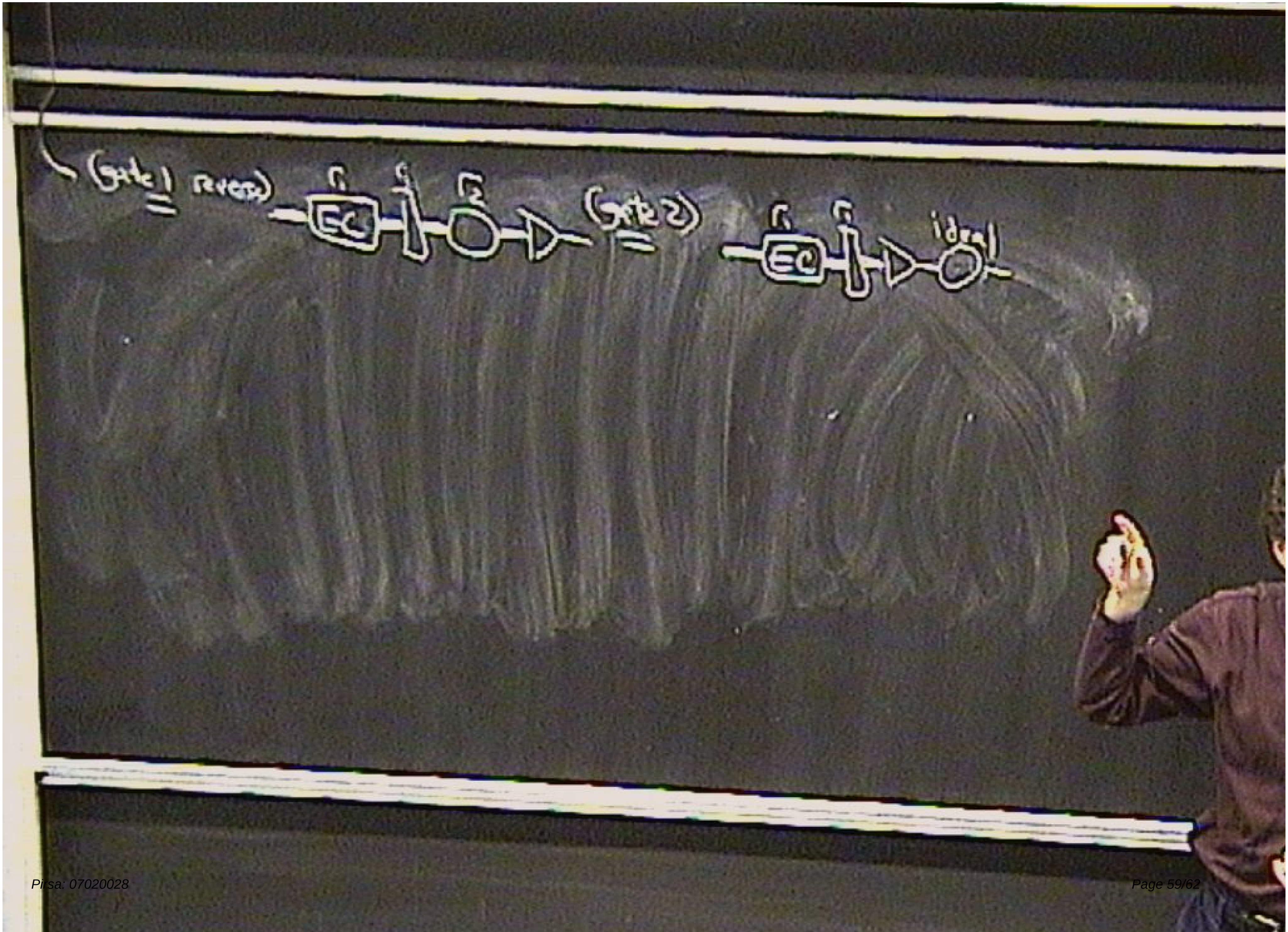
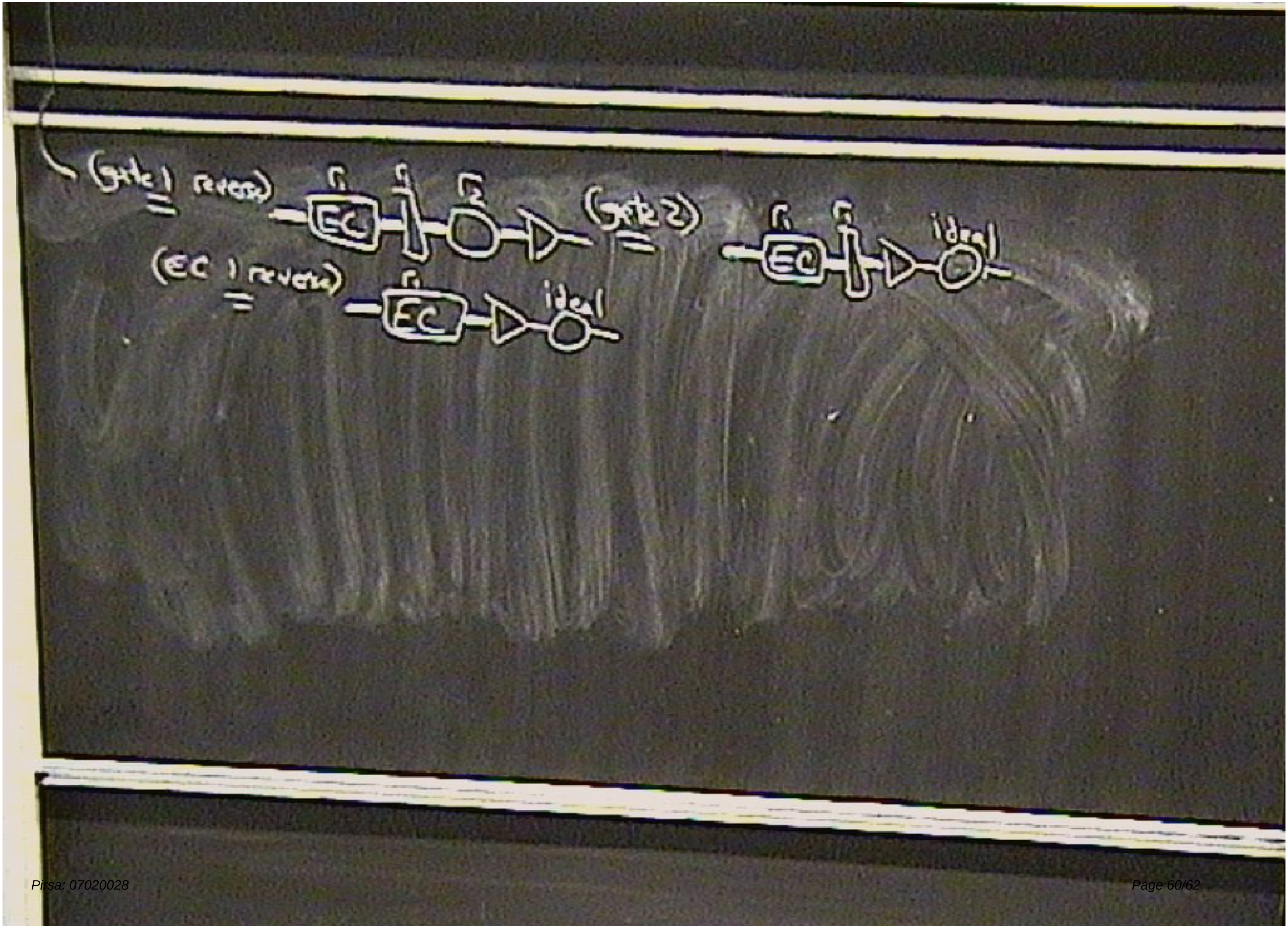
Proof:
on the same qubit at the same time


(gate 1 reverse)
EC
(gate 2)
EC
ideal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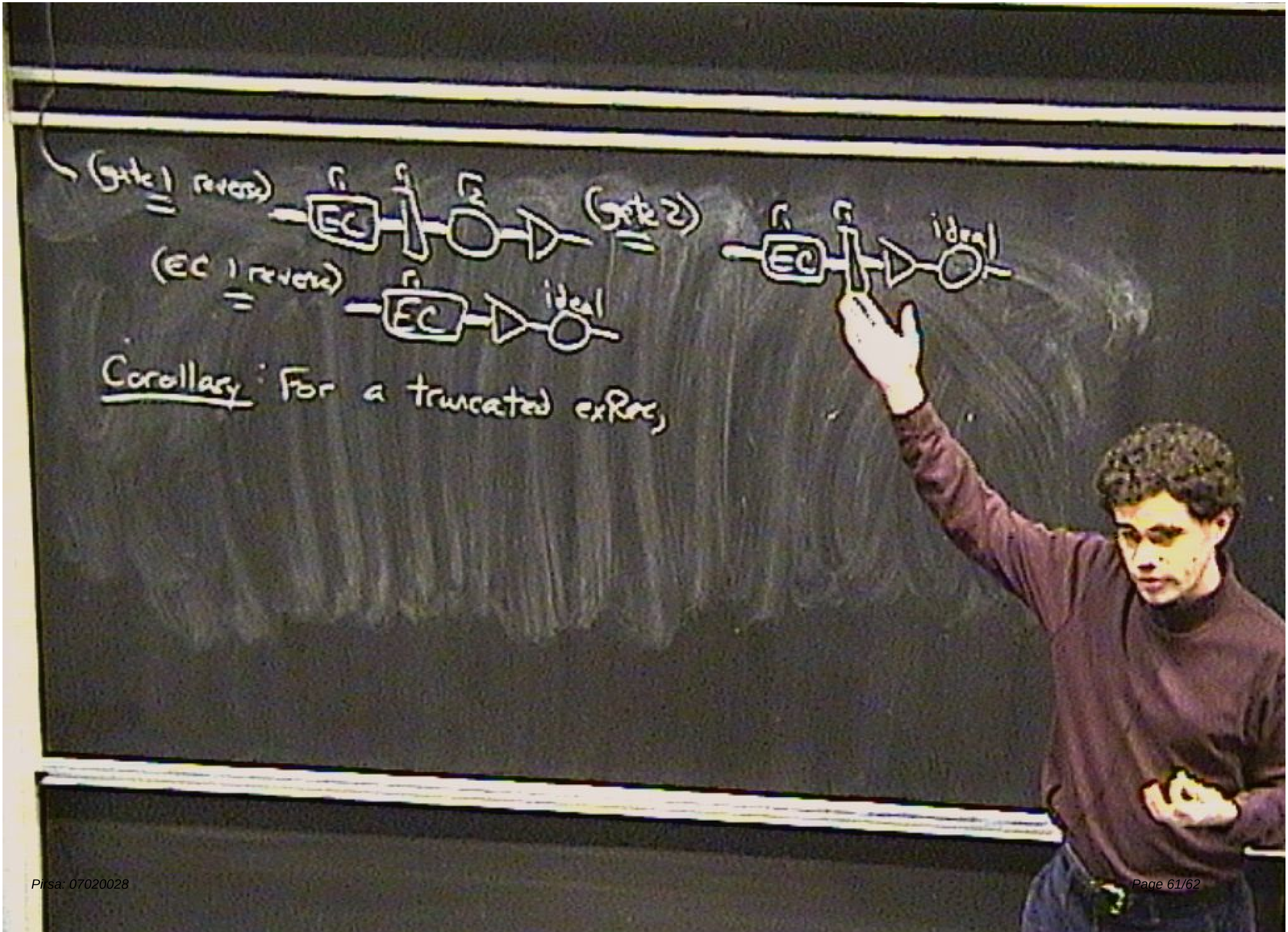
(gate 1 reverse) =
EC
(gate 2) =
EC
ideal
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EC
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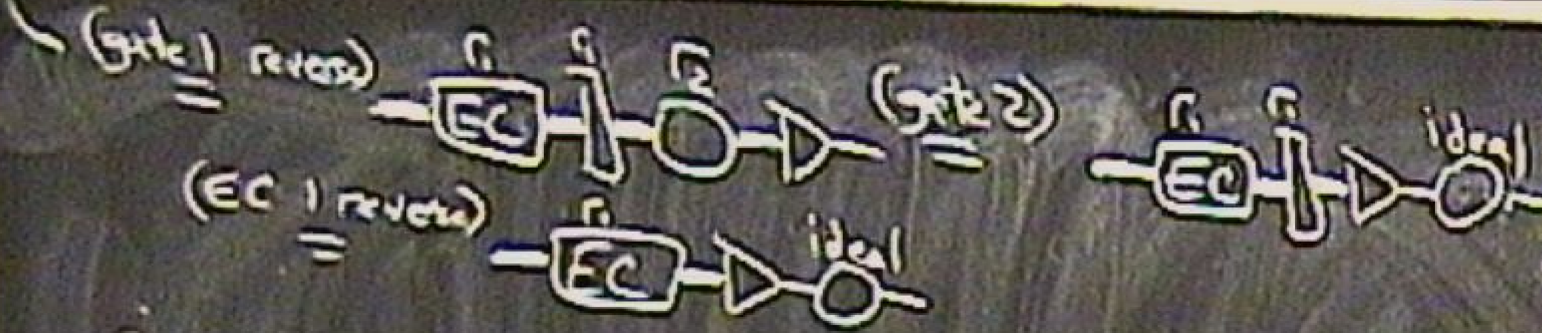
Corollary: For a truncated exRec,



<u>Corollary</u>: For a truncated exRec, good ⇒ correct.

Proof: Insert EC steps w/ no errors to replace truncated ones.